FIG. 1

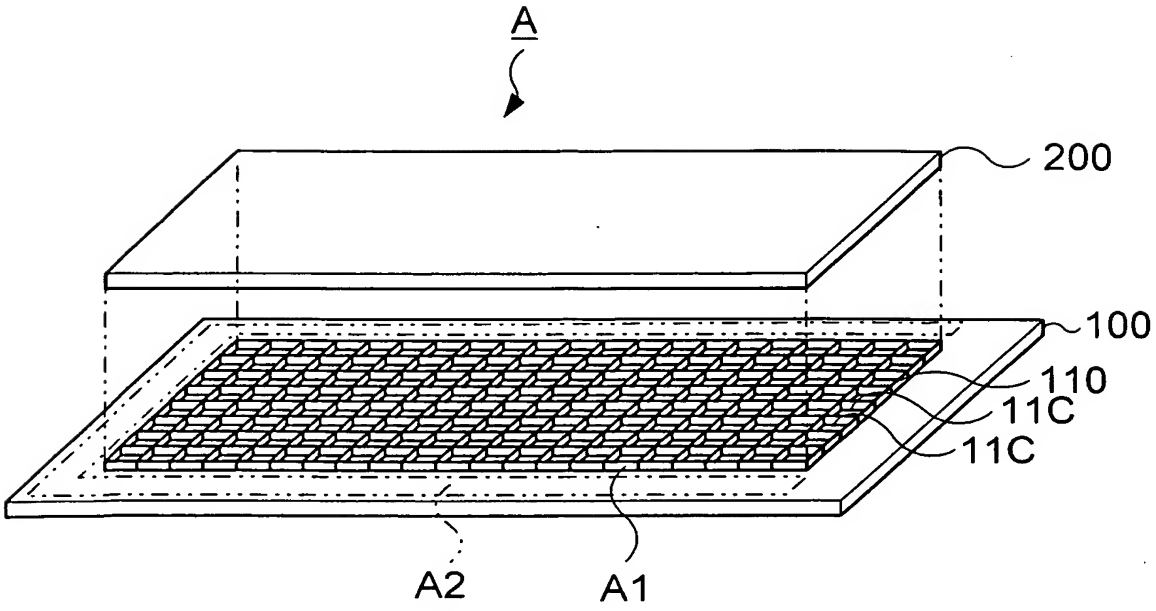
A
200
100
110
11C
11C
A2
A1

FIG. 2

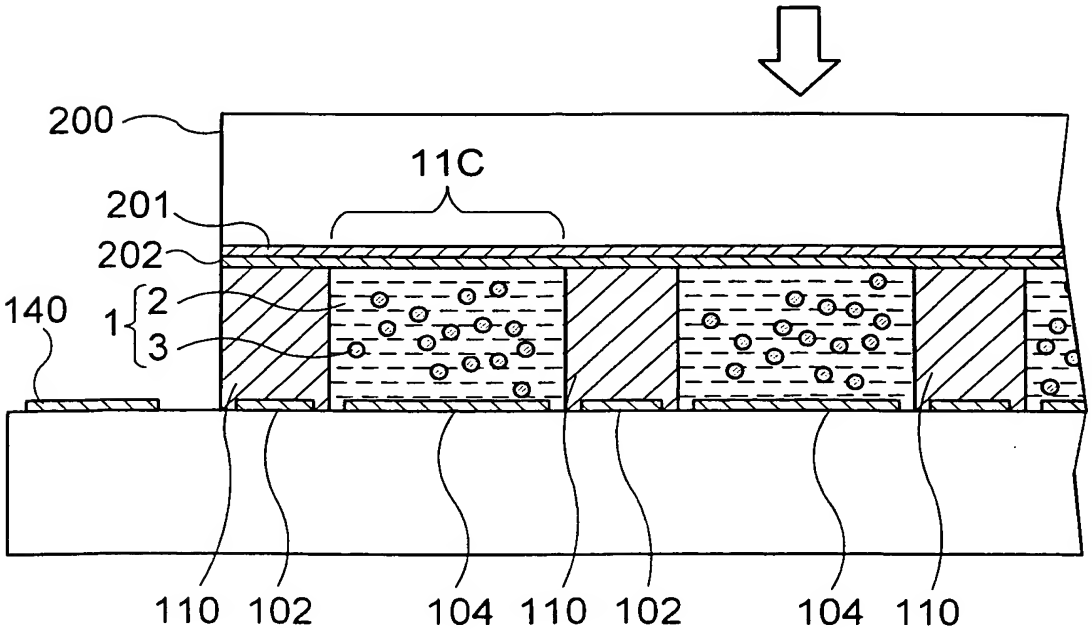
200
11C
201
202
140
1
2
3
110
102
104
110
102
104
110

FIG. 3

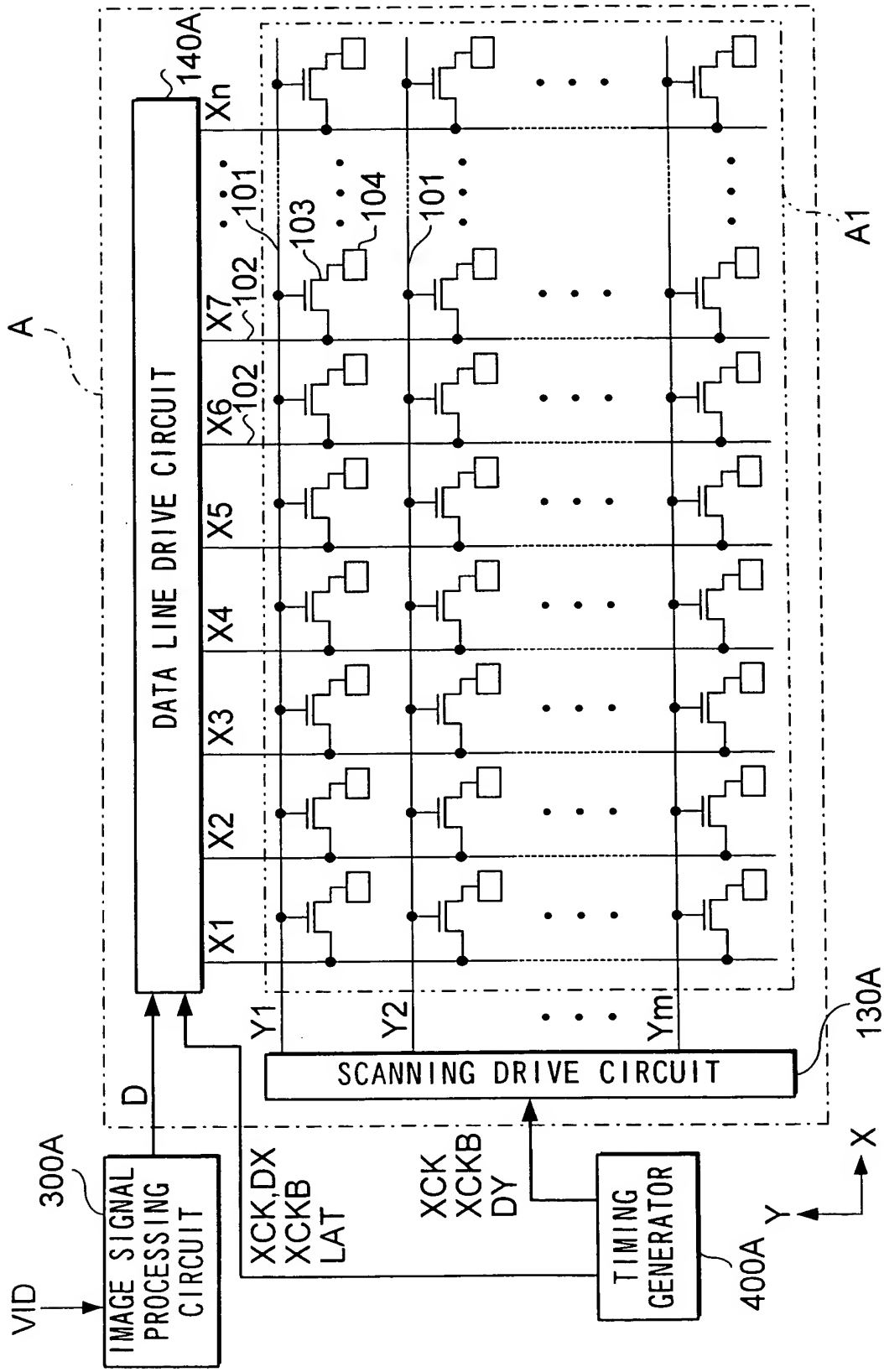
A
140A
DATA LINE DRIVE CIRCUIT
Xn
X7
X6
X5
X4
X3
X2
X1
101
102
103
104
A1
Y1
Y2
Ym
SCANNING DRIVE CIRCUIT
130A
D
300A
IMAGE SIGNAL PROCESSING CIRCUIT
VID
XCK,DX
XCKB
LAT
XCK
XCKB
DY
TIMING GENERATOR
400A
Y
X

FIG. 4

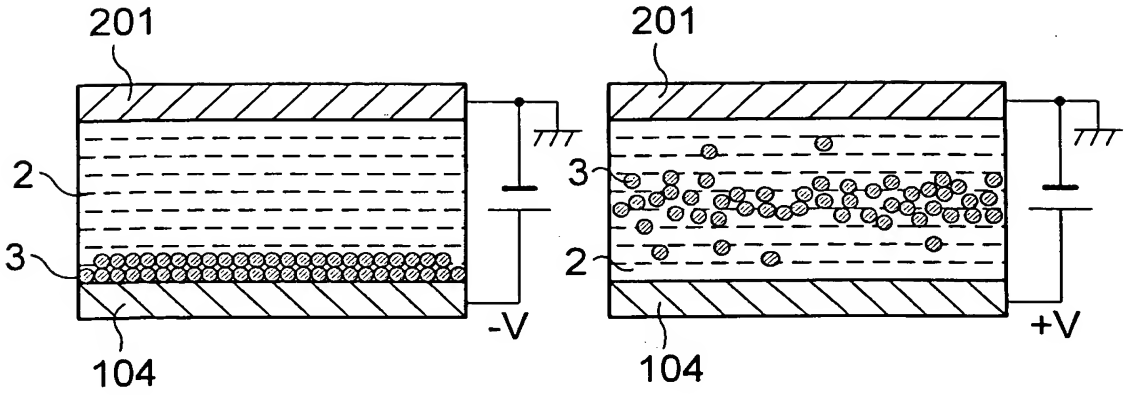
201
201
2
3
3
2
-V
+V
104
104

FIG. 5

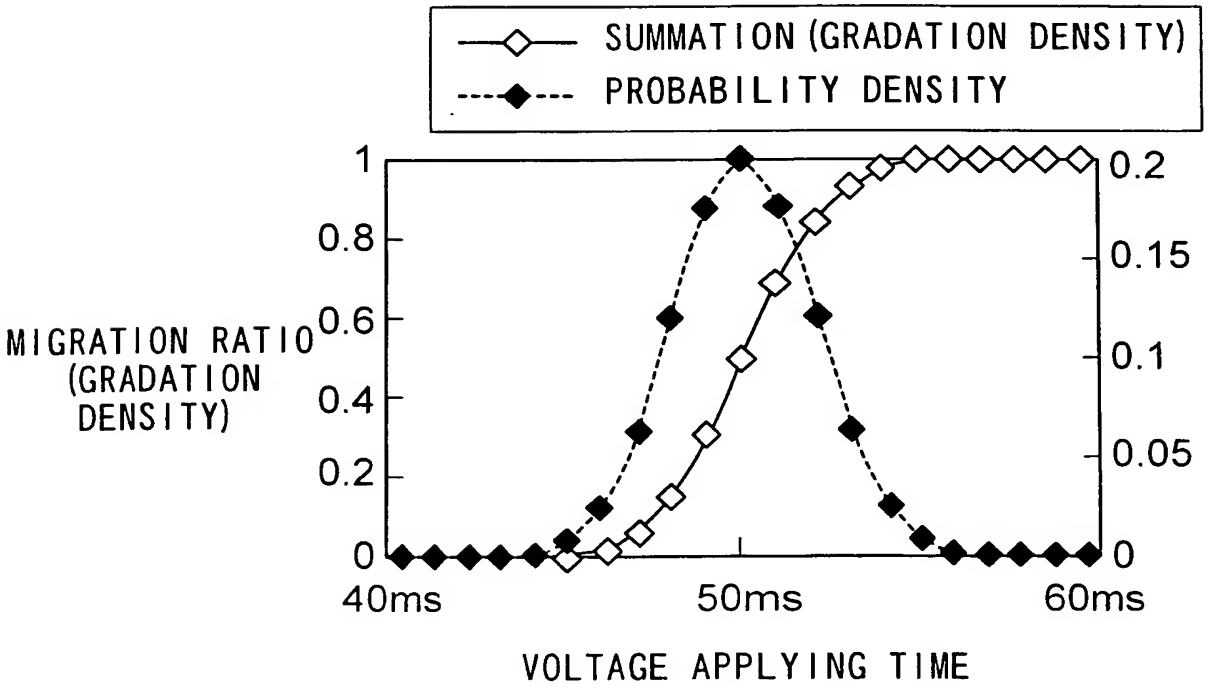
SUMMATION (GRADATION DENSITY)
PROBABILITY DENSITY
MIGRATION RATIO (GRADATION DENSITY)
1
0.8
0.6
0.4
0.2
0
0.2
0.15
0.1
0.05
0
40ms
50ms
60ms
VOLTAGE APPLYING TIME

FIG. 6

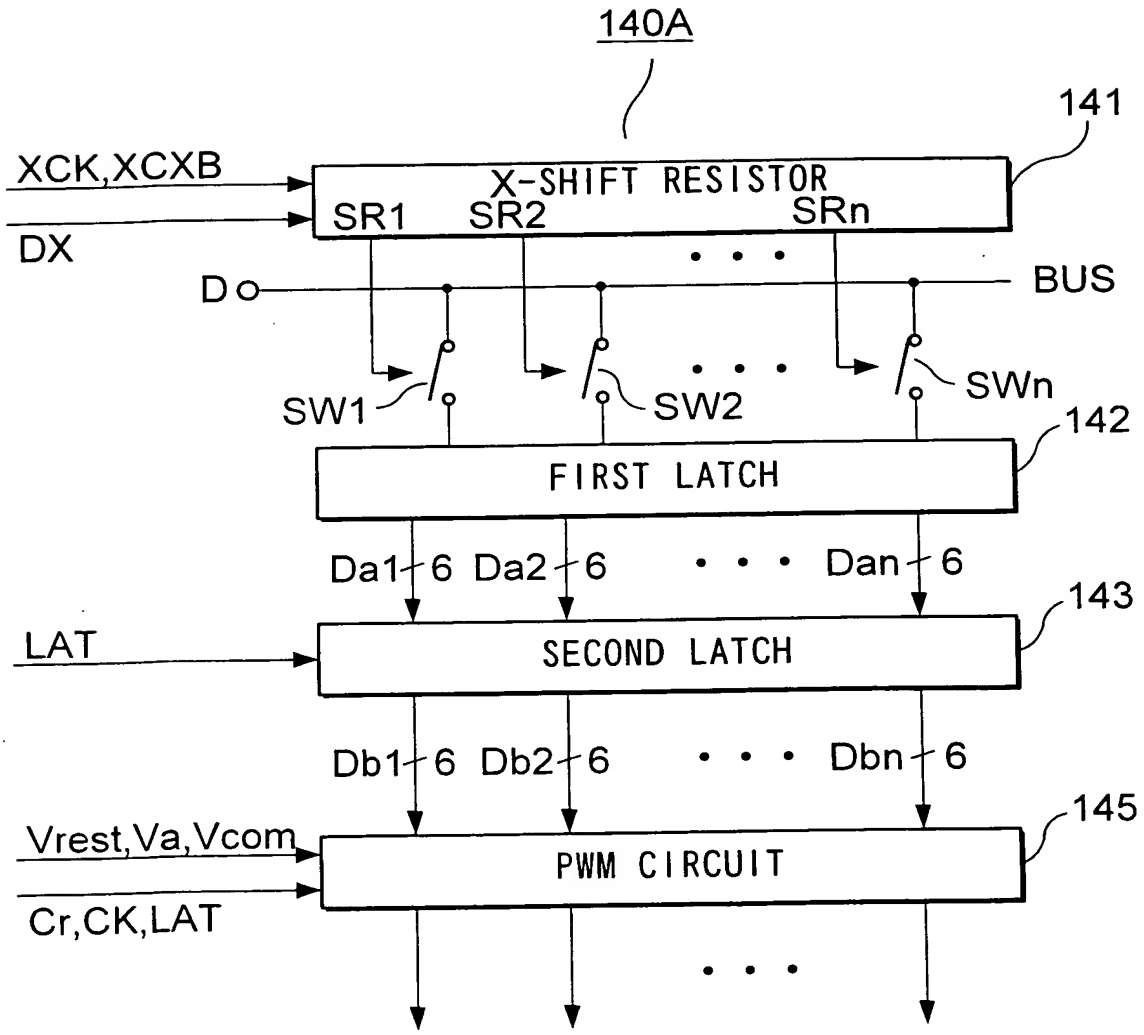
140A
141
XCK,XCXB
DX
X-SHIFT RESISTOR
SR1
SR2
SRn
D
BUS
SW1
SW2
SWn
142
FIRST LATCH
Da1
6
Da2
6
Dan
6
143
LAT
SECOND LATCH
Db1
6
Db2
6
Dbn
6
145
Vrest,Va,Vcom
Cr,CK,LAT
PWM CIRCUIT

FIG. 7

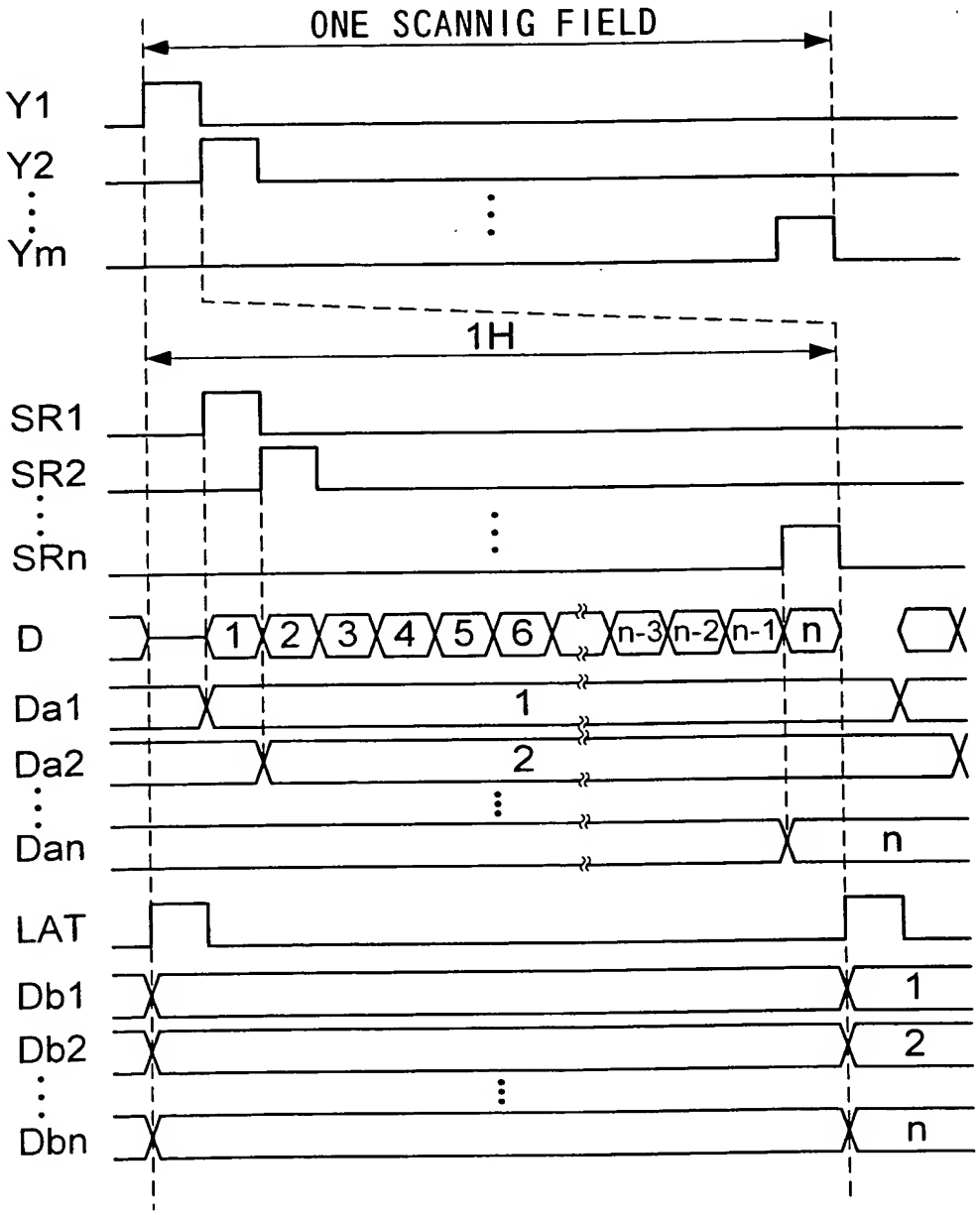
ONE SCANNIG FIELD
Y1
Y2
Ym
1H
SR1
SR2
SRn
D
1
2
3
4
5
6
n-3
n-2
n-1
n
Da1
Da2
Dan
LAT
Db1
Db2
Dbn

FIG. 8

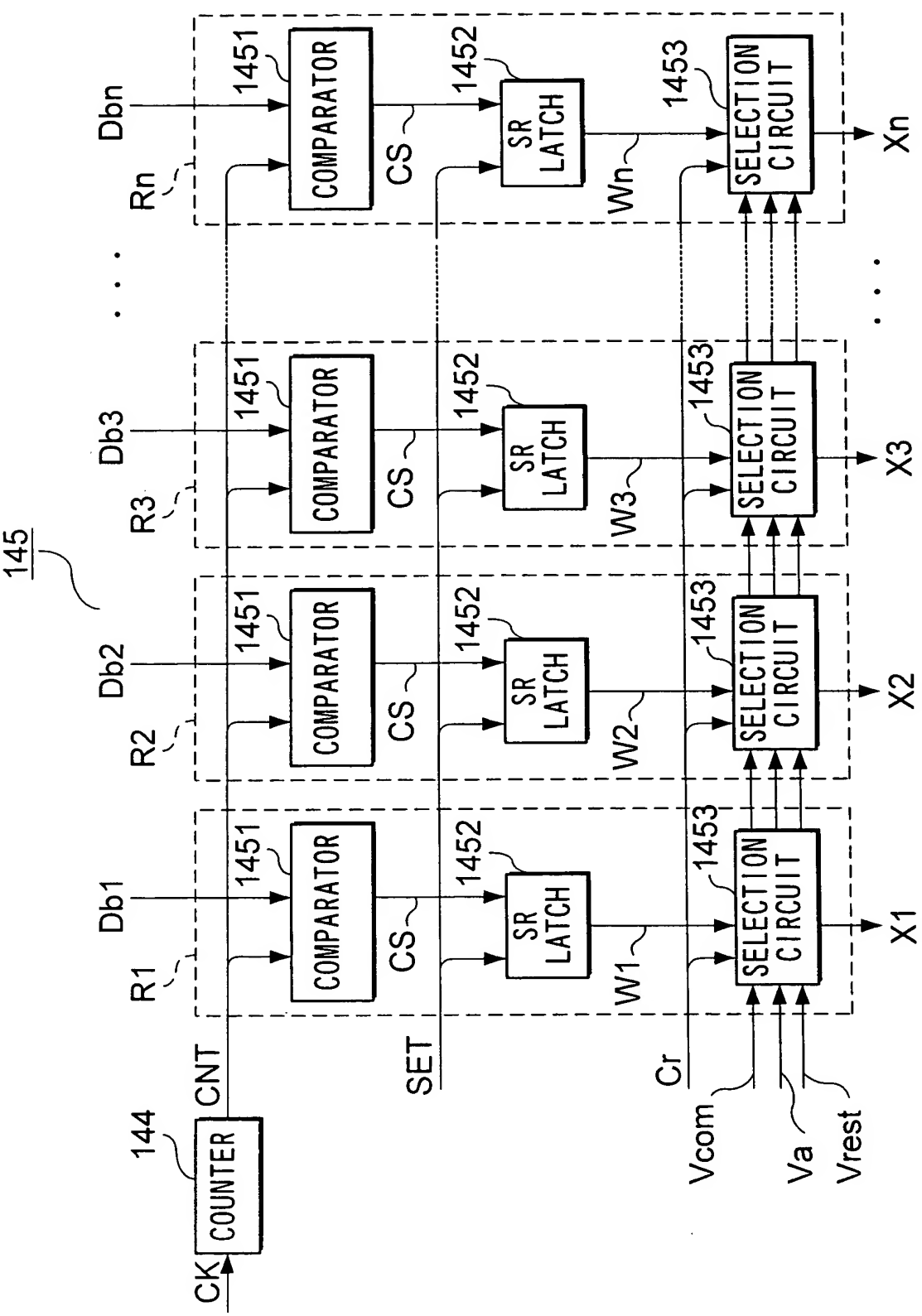
145
144
COUNTER
CK
CNT
SET
Cr
Vcom
Va
Vrest
Db1
Db2
Db3
Dbn
R1
R2
R3
Rn
1451
COMPARATOR
CS
1452
SR LATCH
W1
W2
W3
Wn
1453
SELECTION CIRCUIT
X1
X2
X3
Xn

FIG. 9

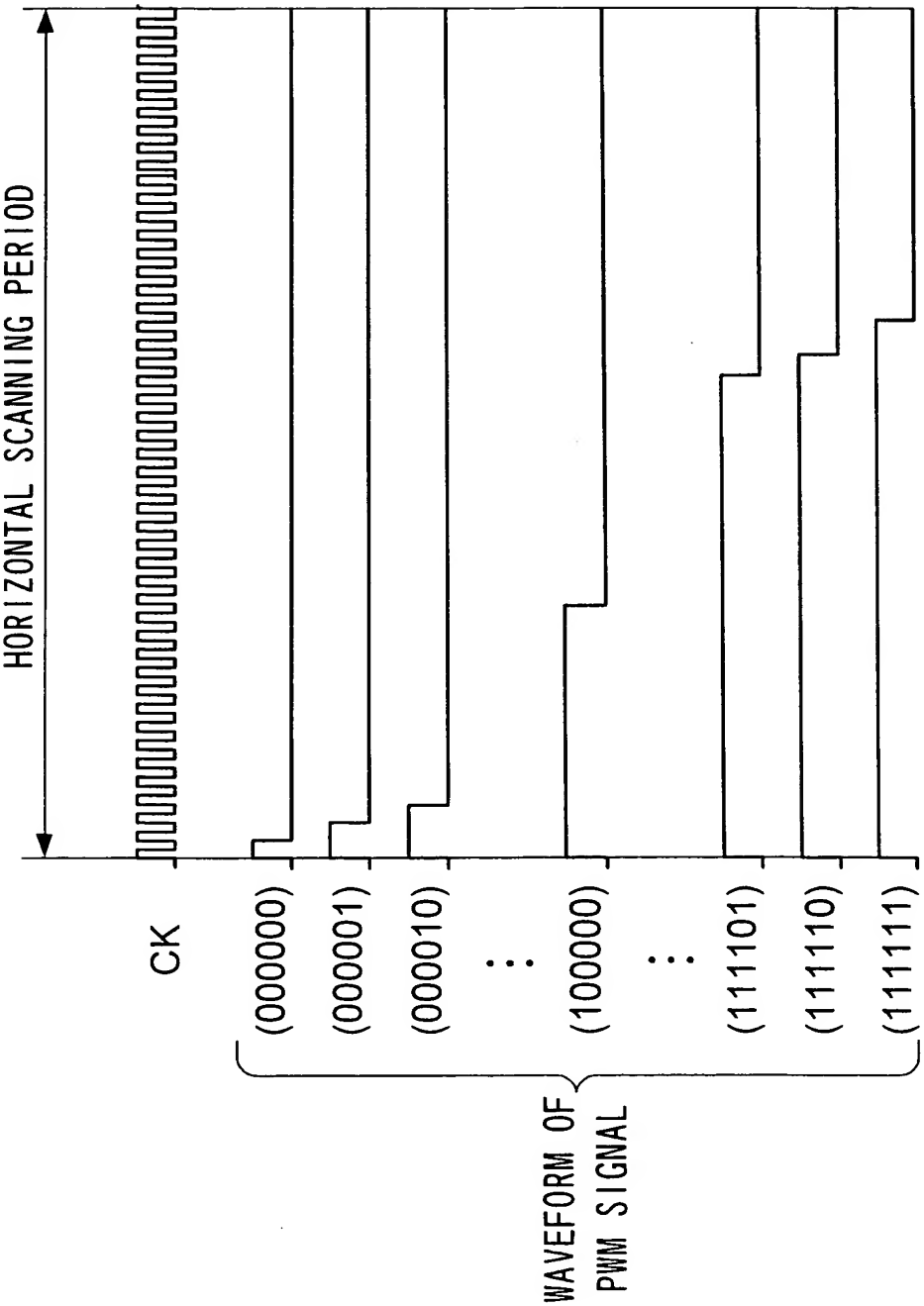
HORIZONTAL SCANNING PERIOD
CK
(000000)
(000001)
(000010)
...
(100000)
...
(111101)
(111110)
(111111)
WAVEFORM OF PWM SIGNAL

FIG. 10

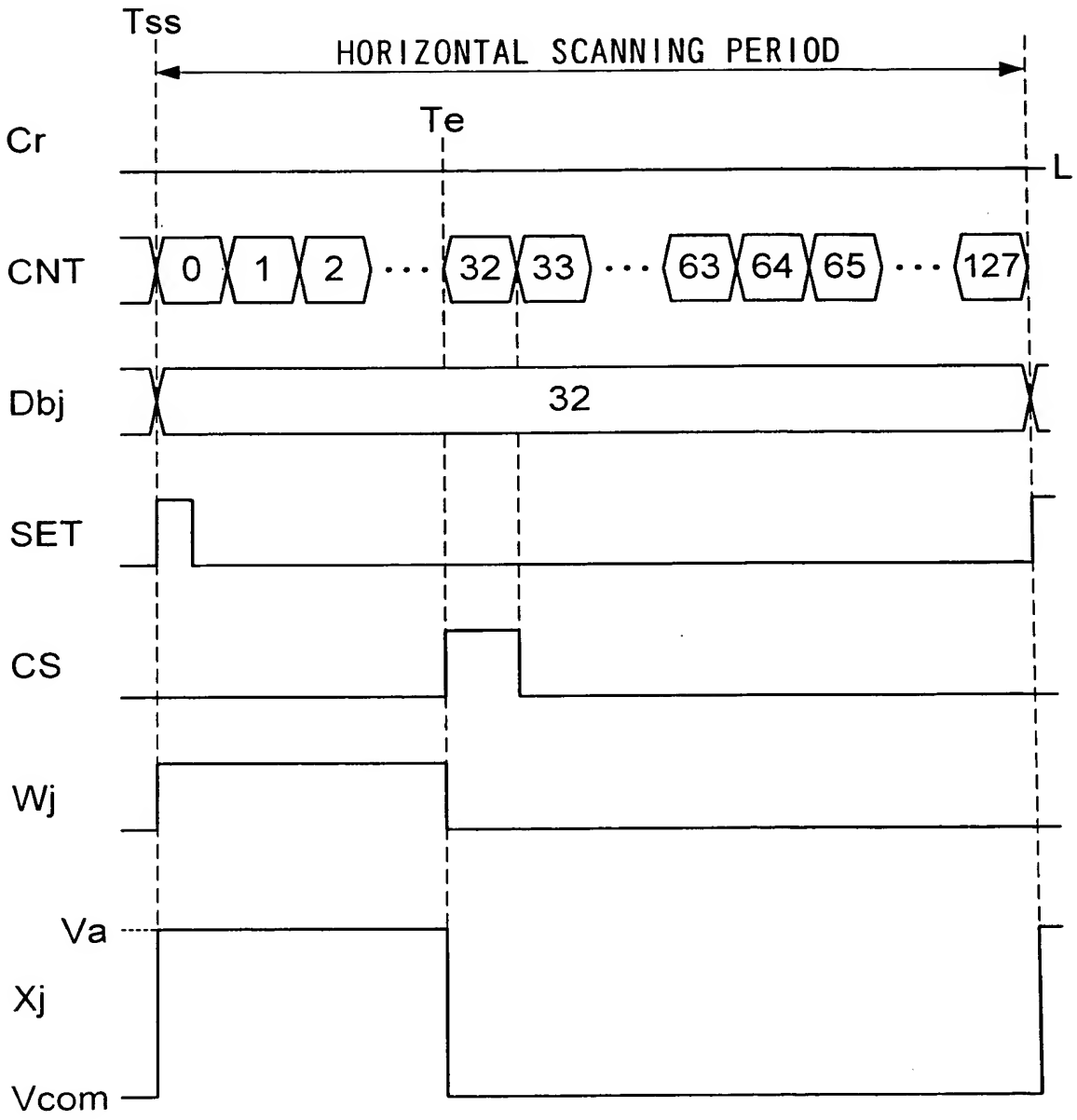
Tss
HORIZONTAL SCANNING PERIOD
Te
Cr
L
CNT
0
1
2
32
33
63
64
65
127
Dbj
32
SET
CS
Wj
Va
Xj
Vcom

FIG. 11

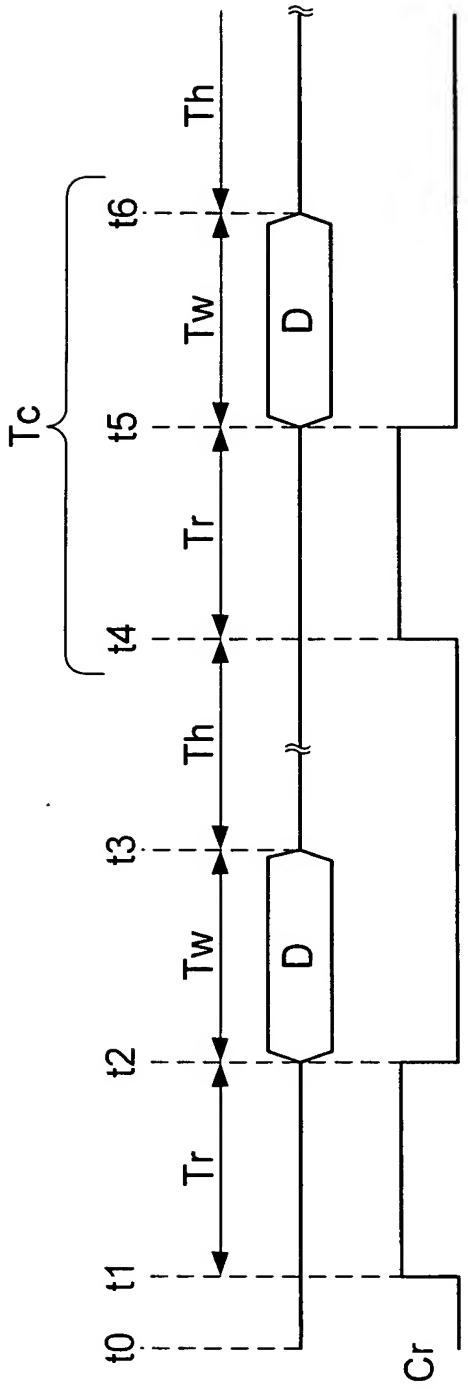

FIG. 12

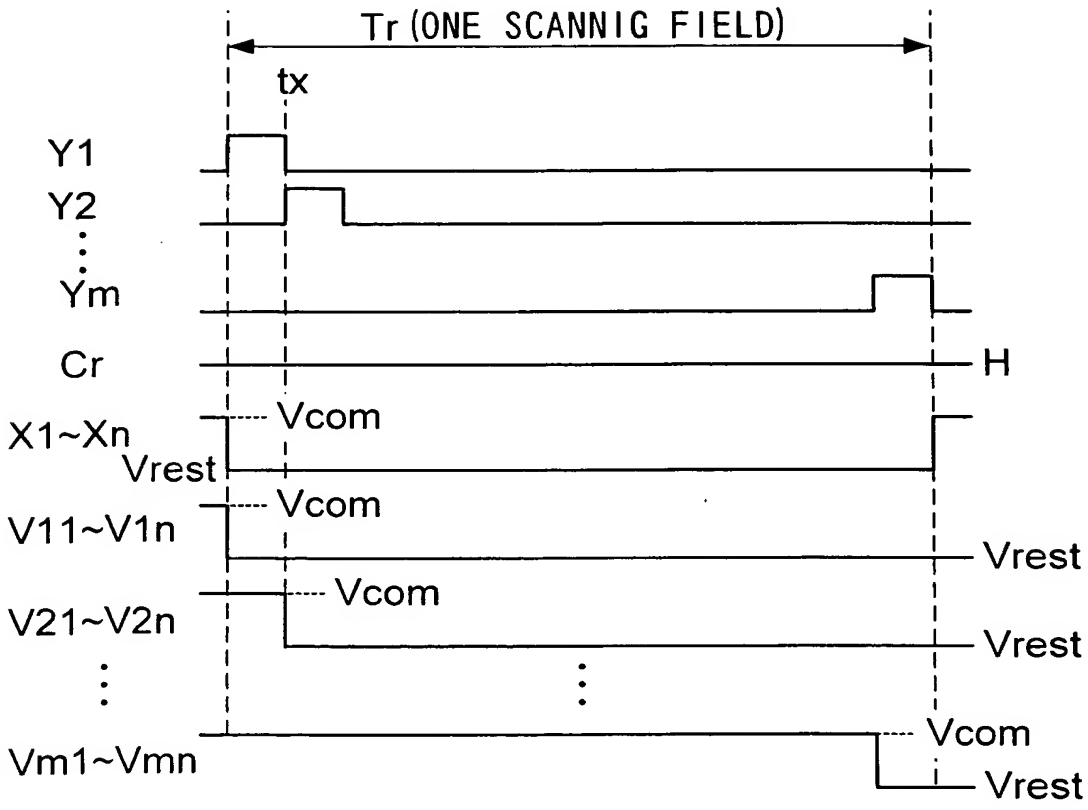
Tr (ONE SCANNIG FIELD)
tx
Y1
Y2
Ym
Cr
H
X1~Xn
Vcom
Vrest
V11~V1n
Vcom
Vrest
V21~V2n
Vcom
Vrest
Vm1~Vmn
Vcom
Vrest

FIG. 13

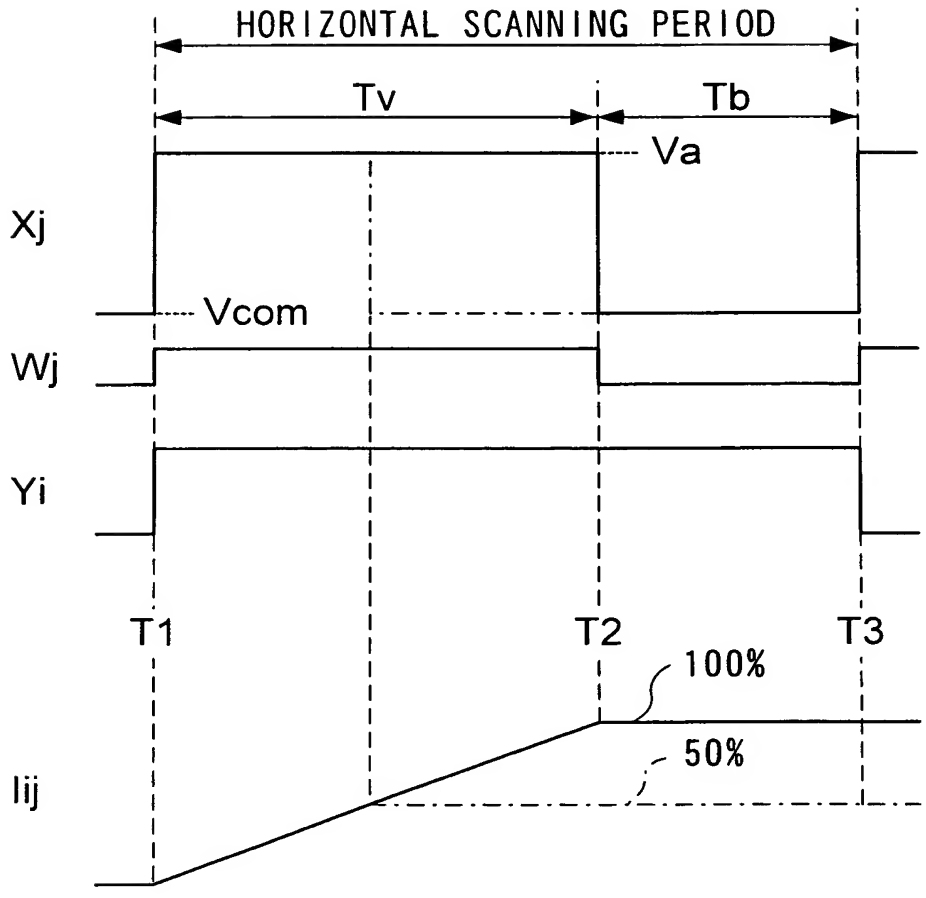
HORIZONTAL SCANNING PERIOD
Tv
Tb
Va
Xj
Vcom
Wj
Yi
T1
T2
T3
100%
50%
Iij

FIG. 14

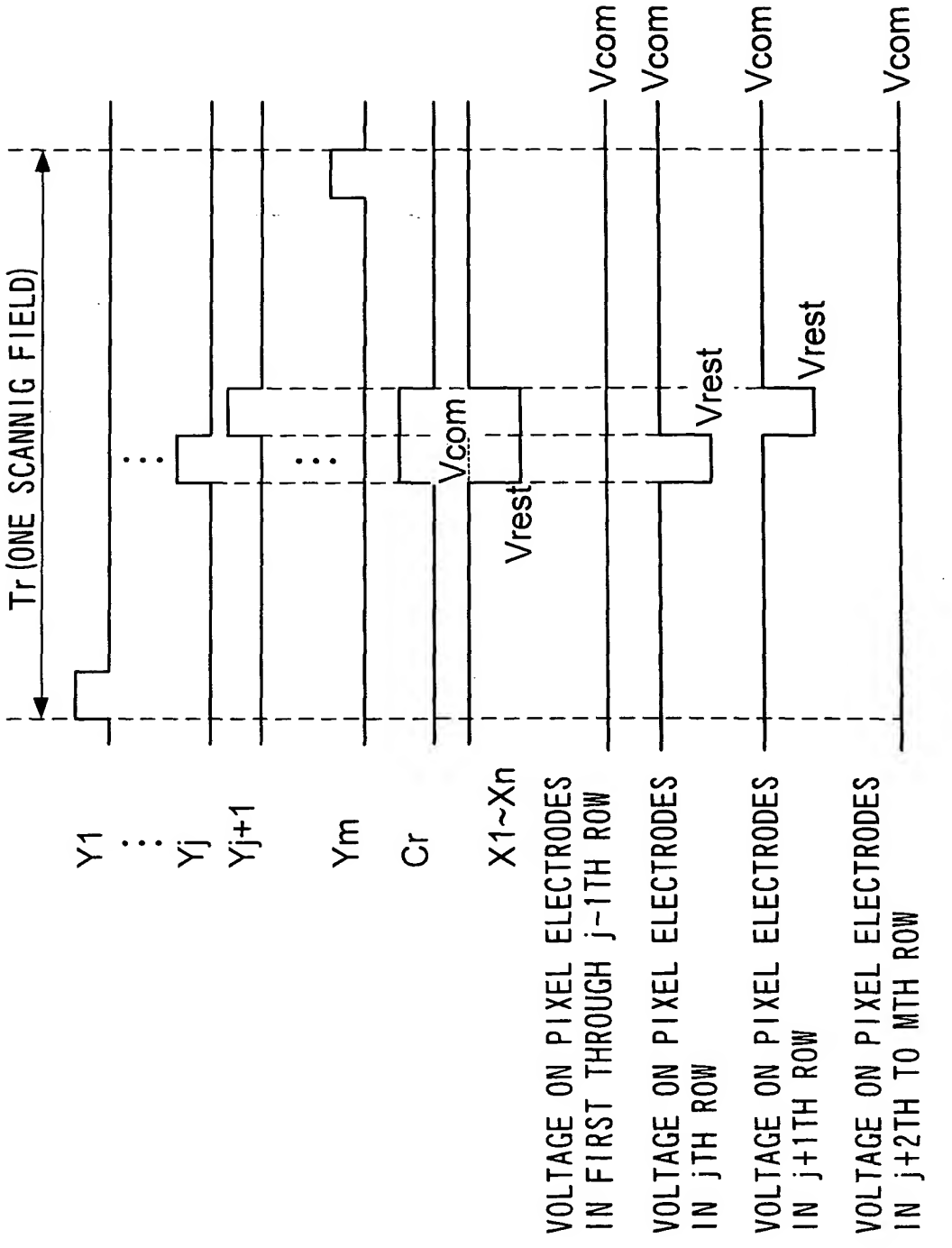
Tr (ONE SCANNIG FIELD)
Y1
Yj
Yj+1
Ym
Cr
X1~Xn
Vcom
Vrest
VOLTAGE ON PIXEL ELECTRODES IN FIRST THROUGH j-1TH ROW
VOLTAGE ON PIXEL ELECTRODES IN jTH ROW
VOLTAGE ON PIXEL ELECTRODES IN j+1TH ROW
VOLTAGE ON PIXEL ELECTRODES IN j+2TH TO MTH ROW

FIG. 15

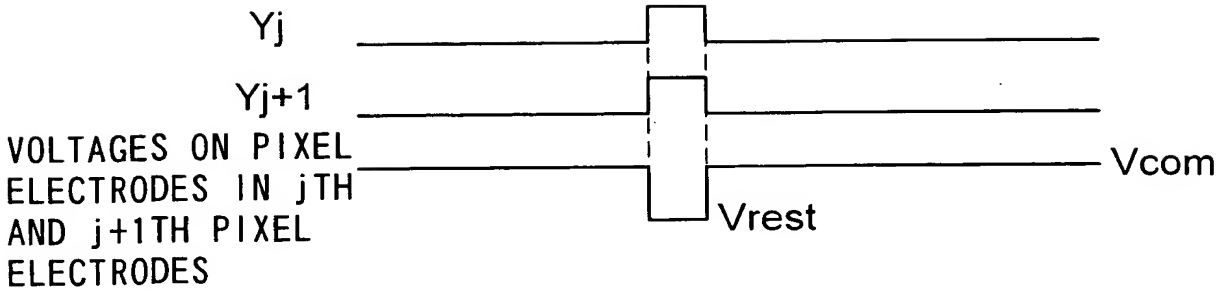
Yj
Yj+1
VOLTAGES ON PIXEL ELECTRODES IN jTH AND j+1TH PIXEL ELECTRODES
Vcom
Vrest

FIG. 16

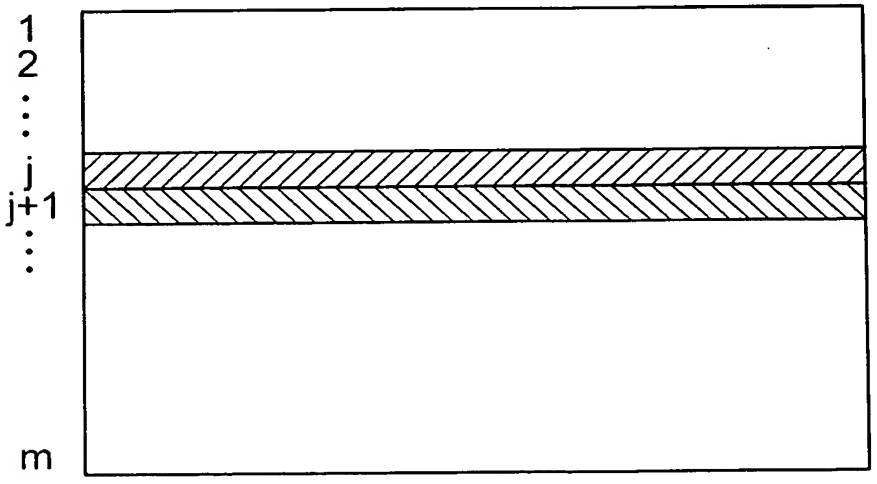
1
2
j
j+1
m

FIG. 17

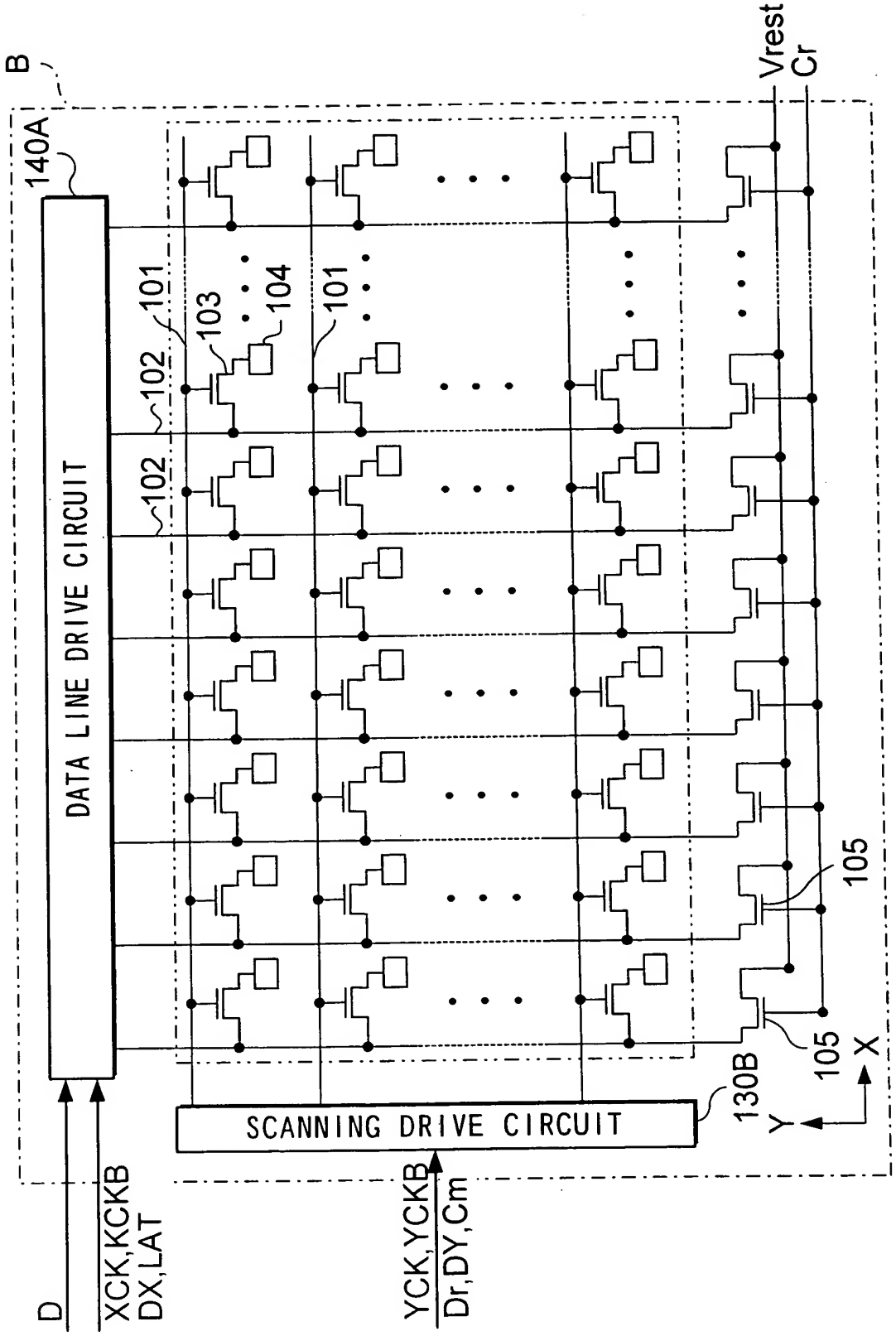
B
140A
DATA LINE DRIVE CIRCUIT
101
102
103
104
Vrest
Cr
105
SCANNING DRIVE CIRCUIT
130B
Y
X
D
XCK,KCKB
DX,LAT
YCK,YCKB
Dr,DY,Cm

FIG. 18

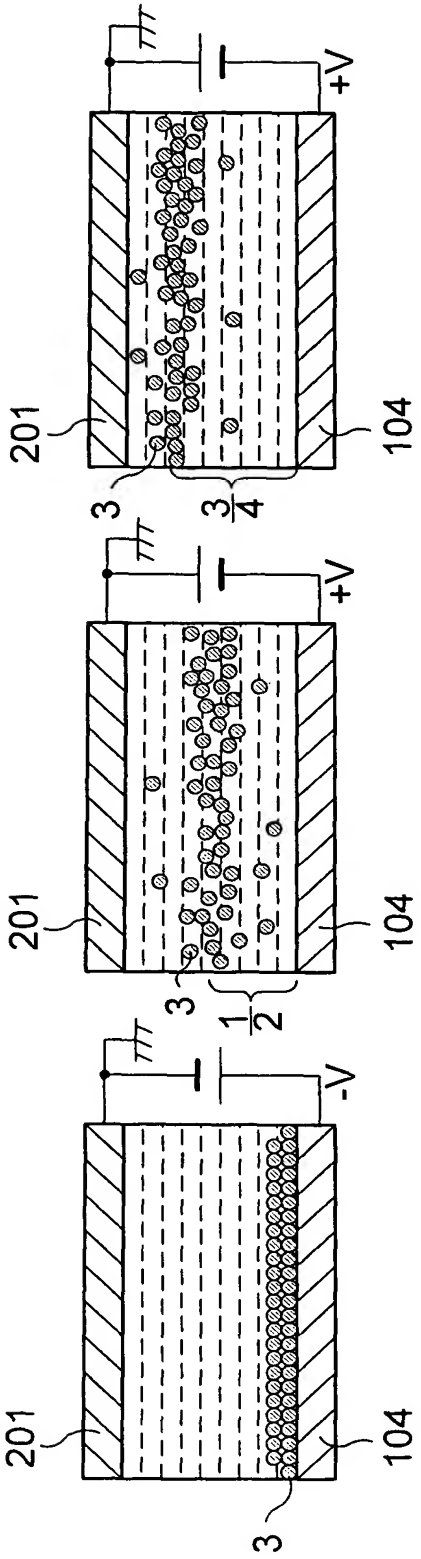

FIG. 19

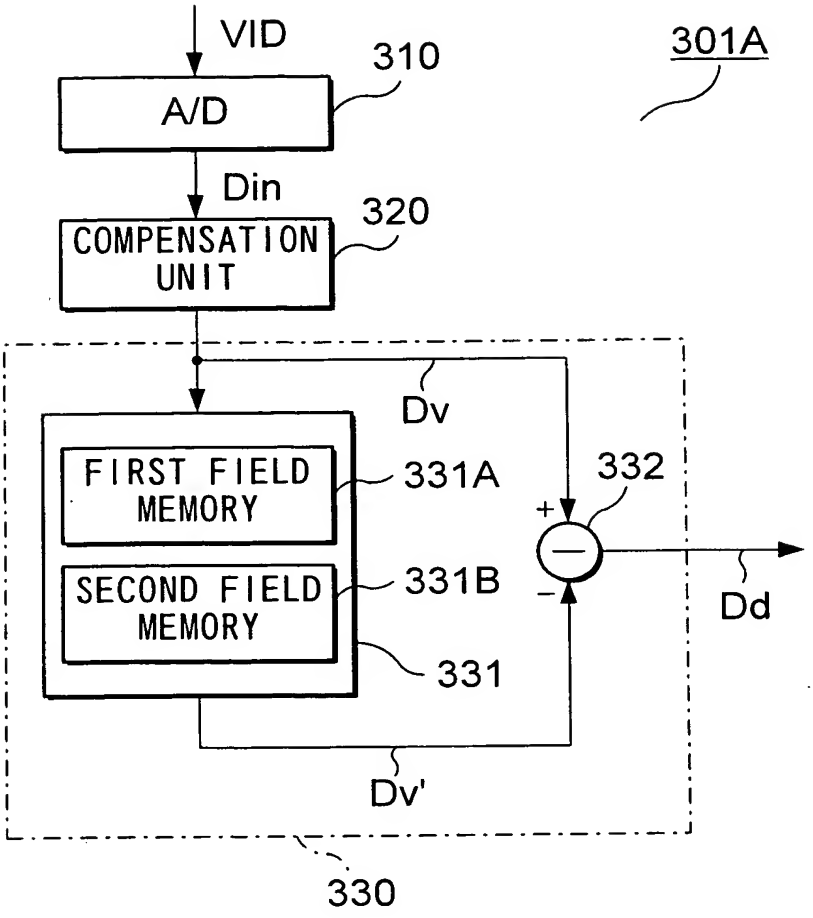
VID
310
301A
A/D
Din
320
COMPENSATION UNIT
Dv
FIRST FIELD MEMORY
331A
332
+
SECOND FIELD MEMORY
331B
−
Dd
331
Dv'
330

FIG. 20

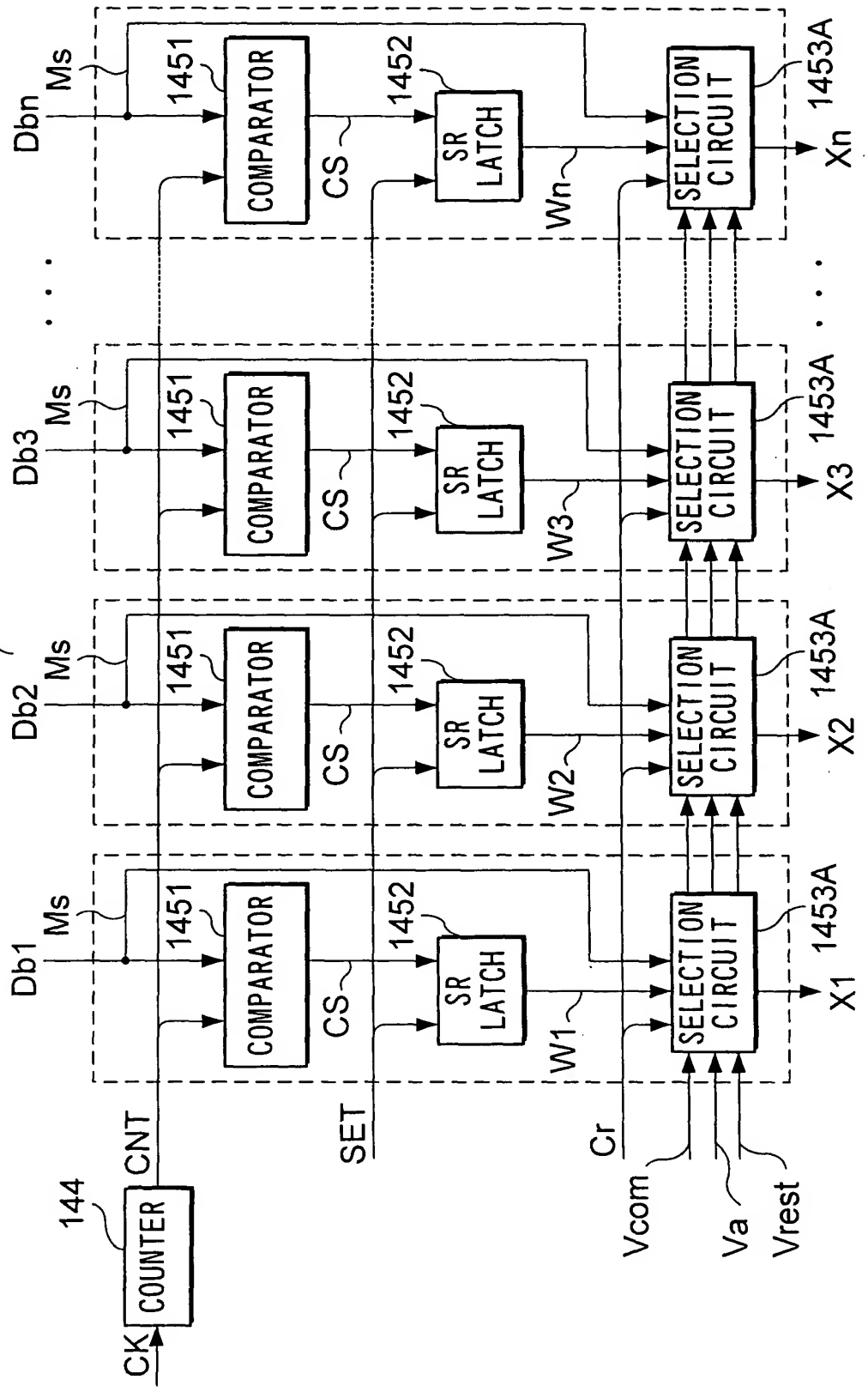
145A
Dbn
Db3
Db2
Db1
Ms
1451
COMPARATOR
CS
1452
SR LATCH
Wn
W3
W2
W1
SELECTION CIRCUIT
1453A
Xn
X3
X2
X1
144
COUNTER
CK
CNT
SET
Cr
Vcom
Va
Vrest

FIG. 21

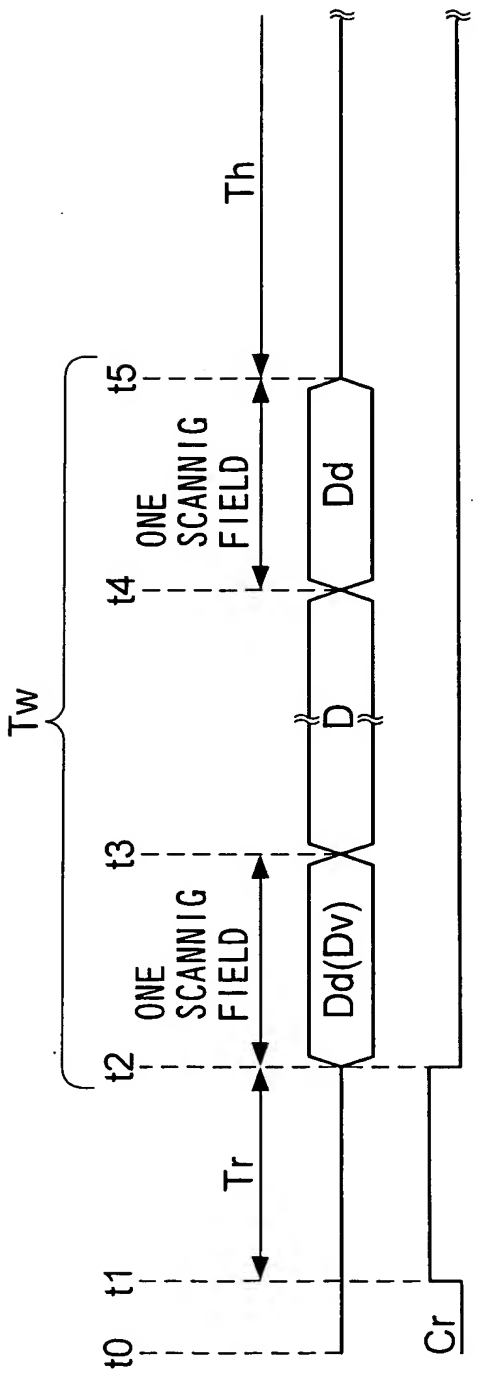
Th
Tw
Tr
t0
t1
t2
t3
t4
t5
ONE SCANNIG FIELD
ONE SCANNIG FIELD
Dd
D
Dd(Dv)
Cr

FIG. 22

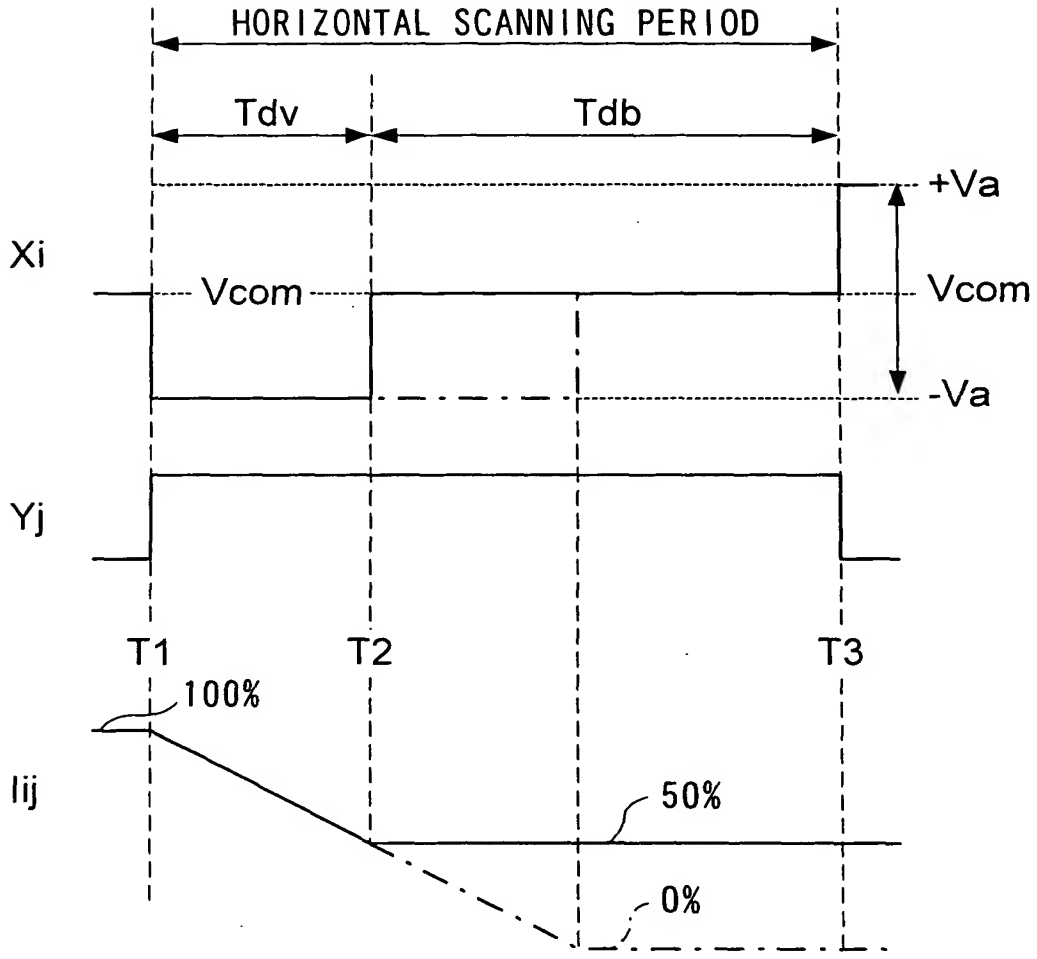
HORIZONTAL SCANNING PERIOD
Tdv
Tdb
+Va
Xi
Vcom
Vcom
-Va
Yj
T1
T2
T3
100%
Iij
50%
0%

FIG. 23

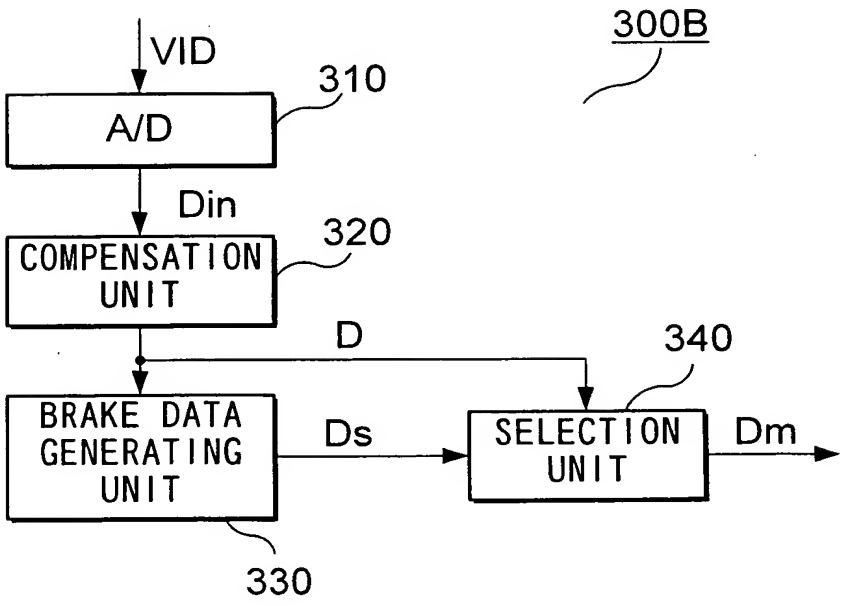
300B
VID
310
A/D
Din
320
COMPENSATION UNIT
D
340
BRAKE DATA GENERATING UNIT
Ds
SELECTION UNIT
Dm
330

FIG. 24

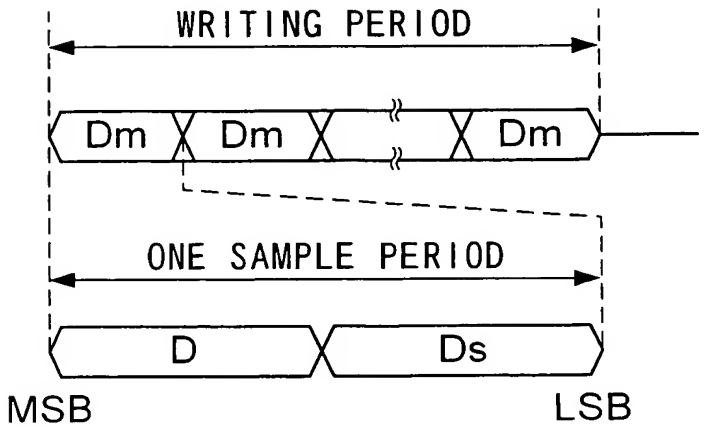
WRITING PERIOD
Dm
Dm
Dm
ONE SAMPLE PERIOD
D
Ds
MSB
LSB

FIG. 25

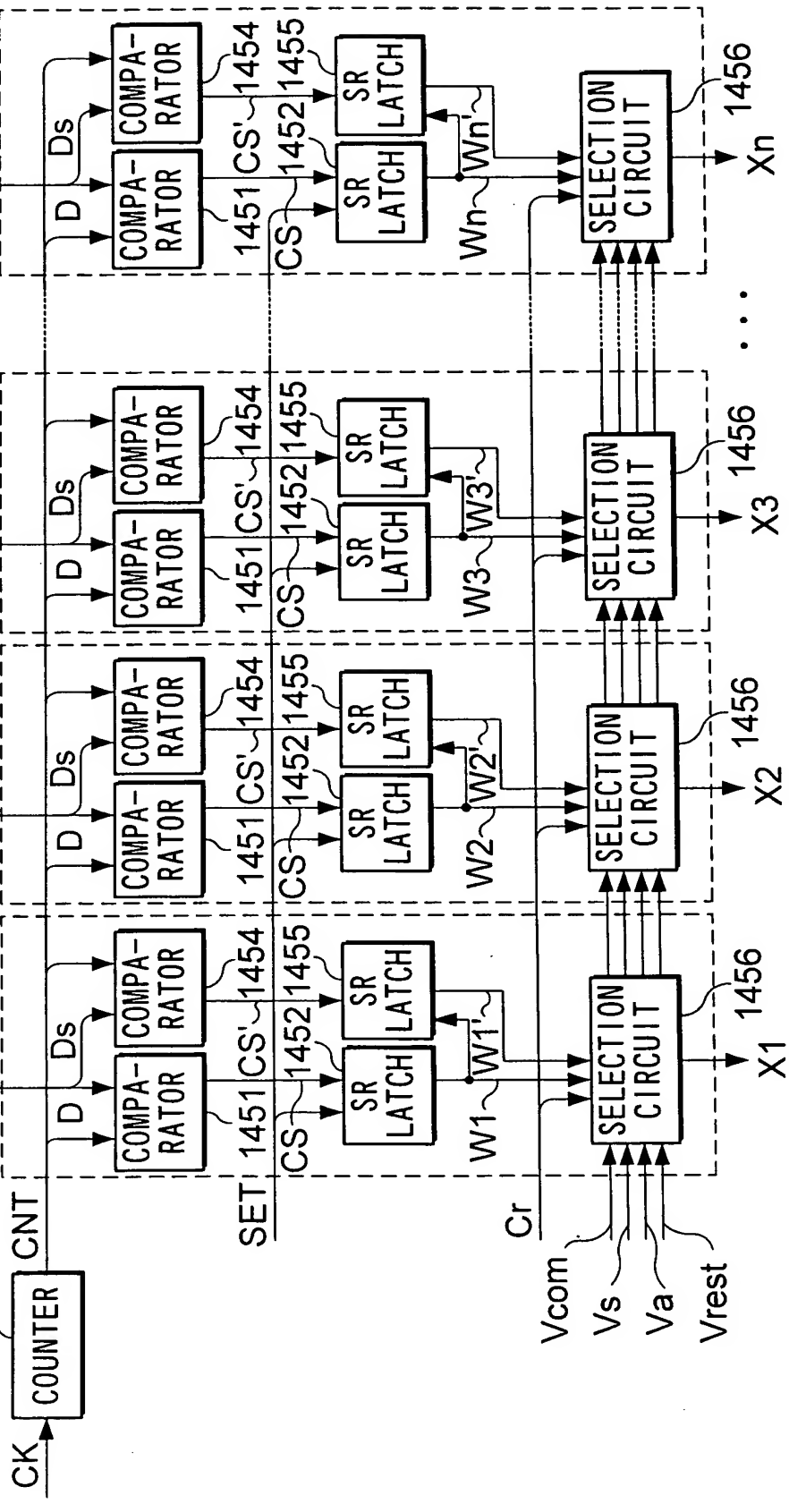
145B
144
COUNTER
CK
CNT
SET
Cr
Vcom
Vs
Va
Vrest
R1
R2
R3
Rn
Db1
Db2
Db3
Dbn
Dm
D
Ds
COMPA-RATOR
1451
1452
CS
CS'
1454
1455
SR LATCH
W1
W2
W3
Wn
W1'
W2'
W3'
Wn'
SELECTION CIRCUIT
1456
X1
X2
X3
Xn

FIG. 26

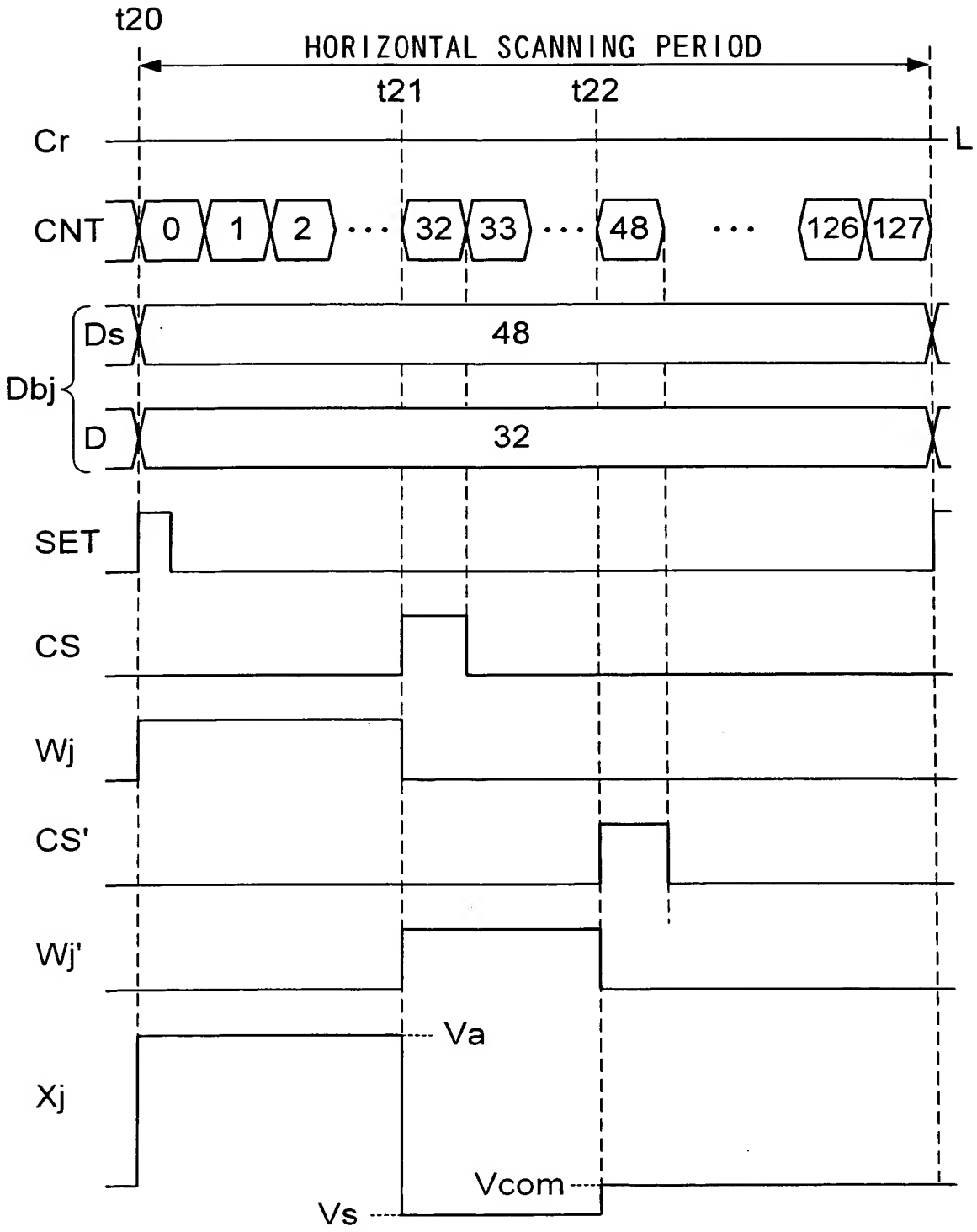
t20
HORIZONTAL SCANNING PERIOD
t21
t22
Cr
L
CNT
0
1
2
32
33
48
126
127
Dbj
Ds
48
D
32
SET
CS
Wj
CS'
Wj'
Va
Xj
Vcom
Vs

FIG. 27

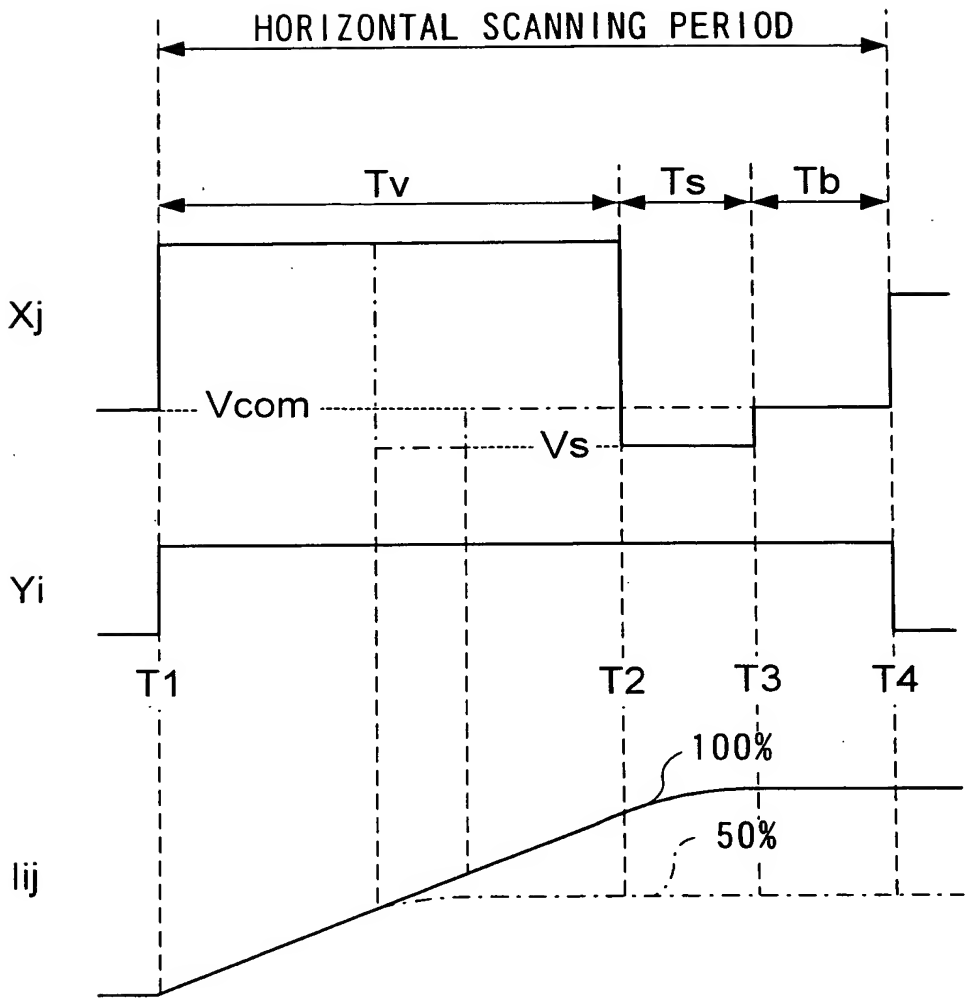
HORIZONTAL SCANNING PERIOD
Tv
Ts
Tb
Xj
Vcom
Vs
Yi
T1
T2
T3
T4
100%
50%
Iij

FIG. 28

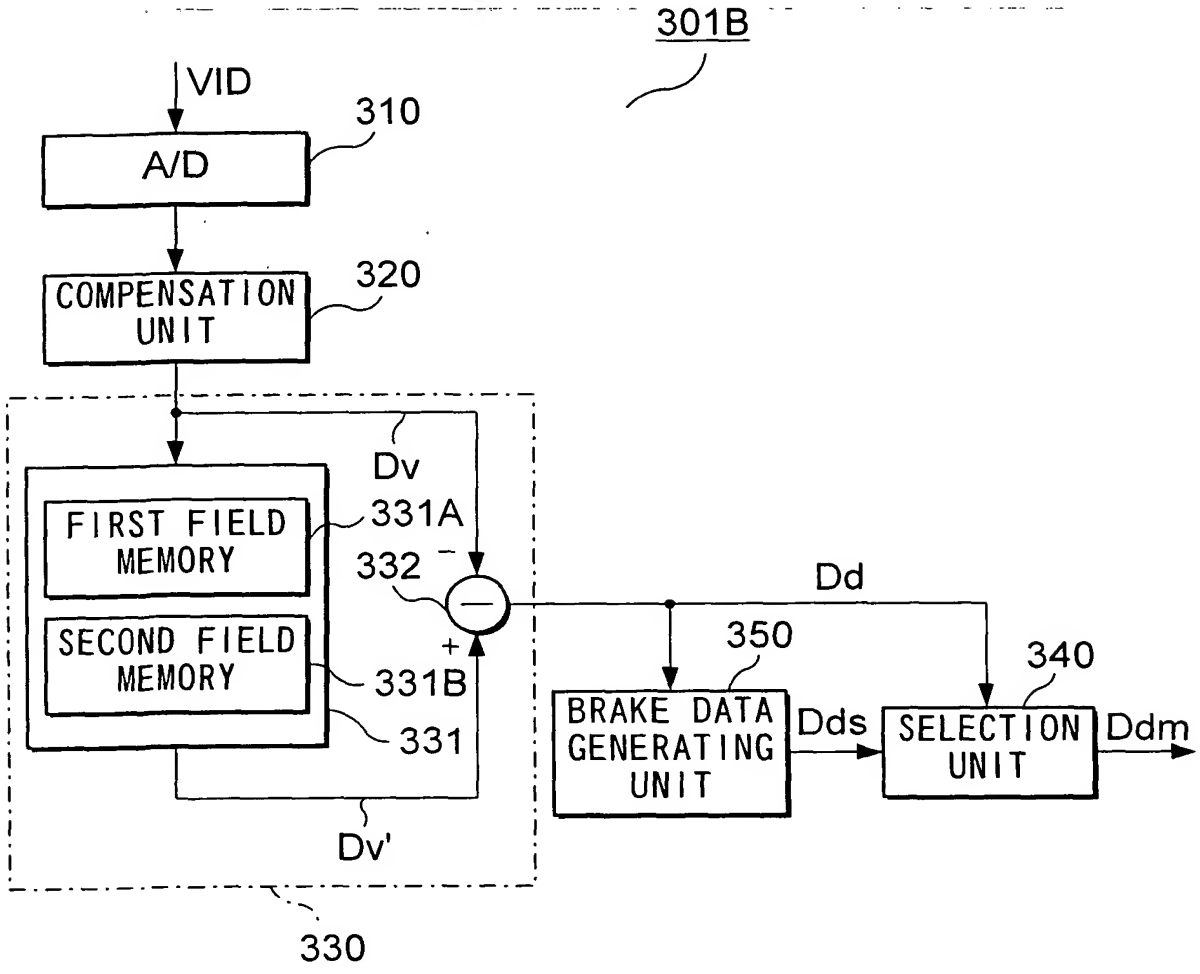
301B
VID
310
A/D
320
COMPENSATION UNIT
Dv
FIRST FIELD MEMORY
331A
332
SECOND FIELD MEMORY
331B
331
Dv'
330
Dd
350
340
BRAKE DATA GENERATING UNIT
Dds
SELECTION UNIT
Ddm

FIG. 29

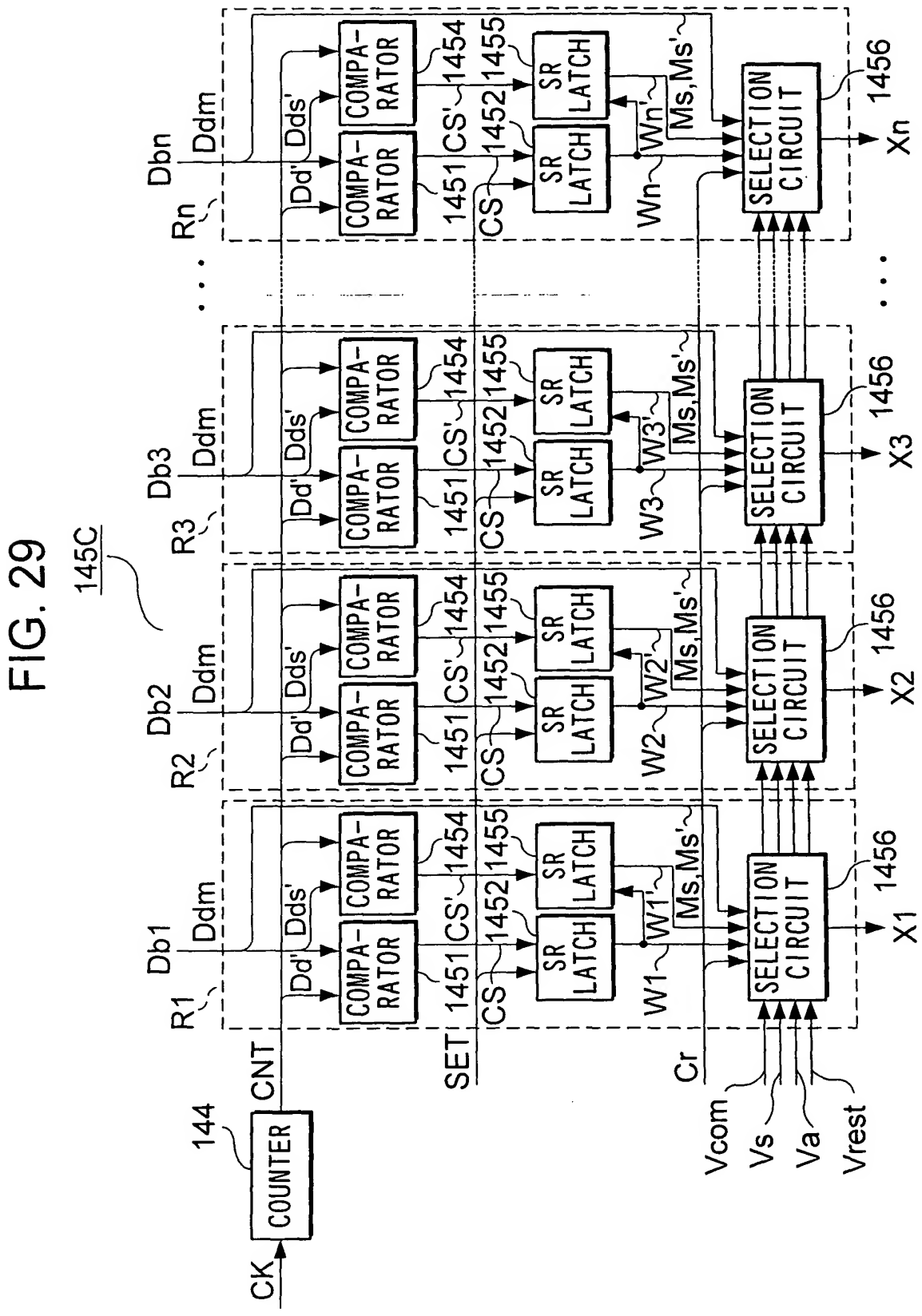
145C
144
COUNTER
CK
CNT
SET
Cr
Vcom
Vs
Va
Vrest
R1
R2
R3
Rn
Db1
Db2
Db3
Dbn
Ddm
Dd'
Dds'
COMPA-RATOR
1451
1452
CS
CS'
SR LATCH
1454
1455
W1
W2
W3
Wn
Ms,Ms'
SELECTION CIRCUIT
1456
X1
X2
X3
Xn

FIG. 30

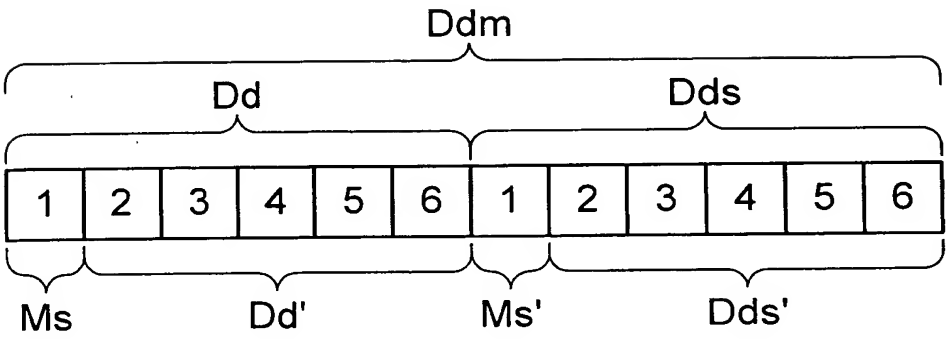

FIG. 31

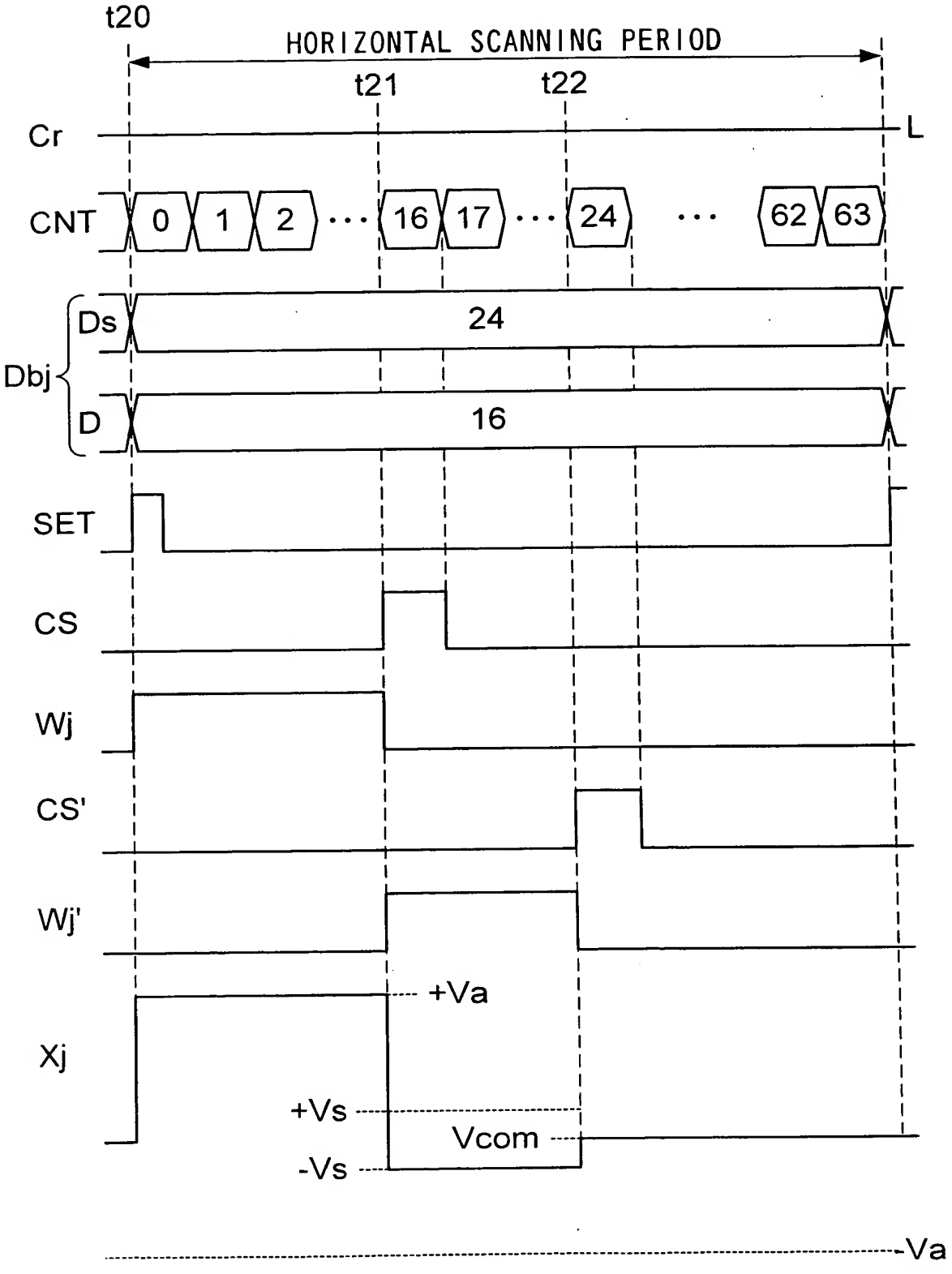
t20
HORIZONTAL SCANNING PERIOD
t21
t22
Cr
L
CNT
0
1
2
16
17
24
62
63
Dbj
Ds
24
D
16
SET
CS
Wj
CS'
Wj'
+Va
Xj
+Vs
Vcom
-Vs
-Va

FIG. 32

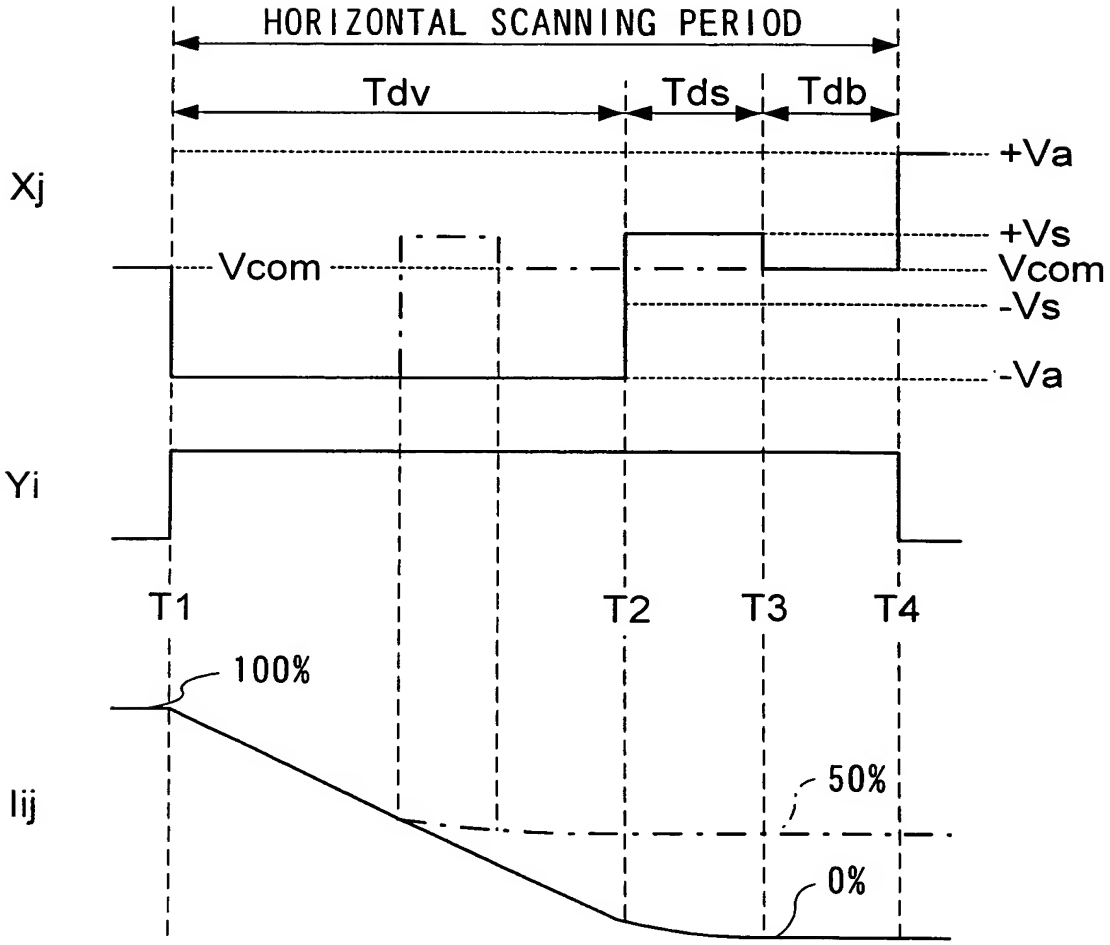
HORIZONTAL SCANNING PERIOD
Tdv
Tds
Tdb
Xj
+Va
+Vs
Vcom
Vcom
-Vs
-Va
Yi
T1
T2
T3
T4
100%
Iij
50%
0%

FIG. 33

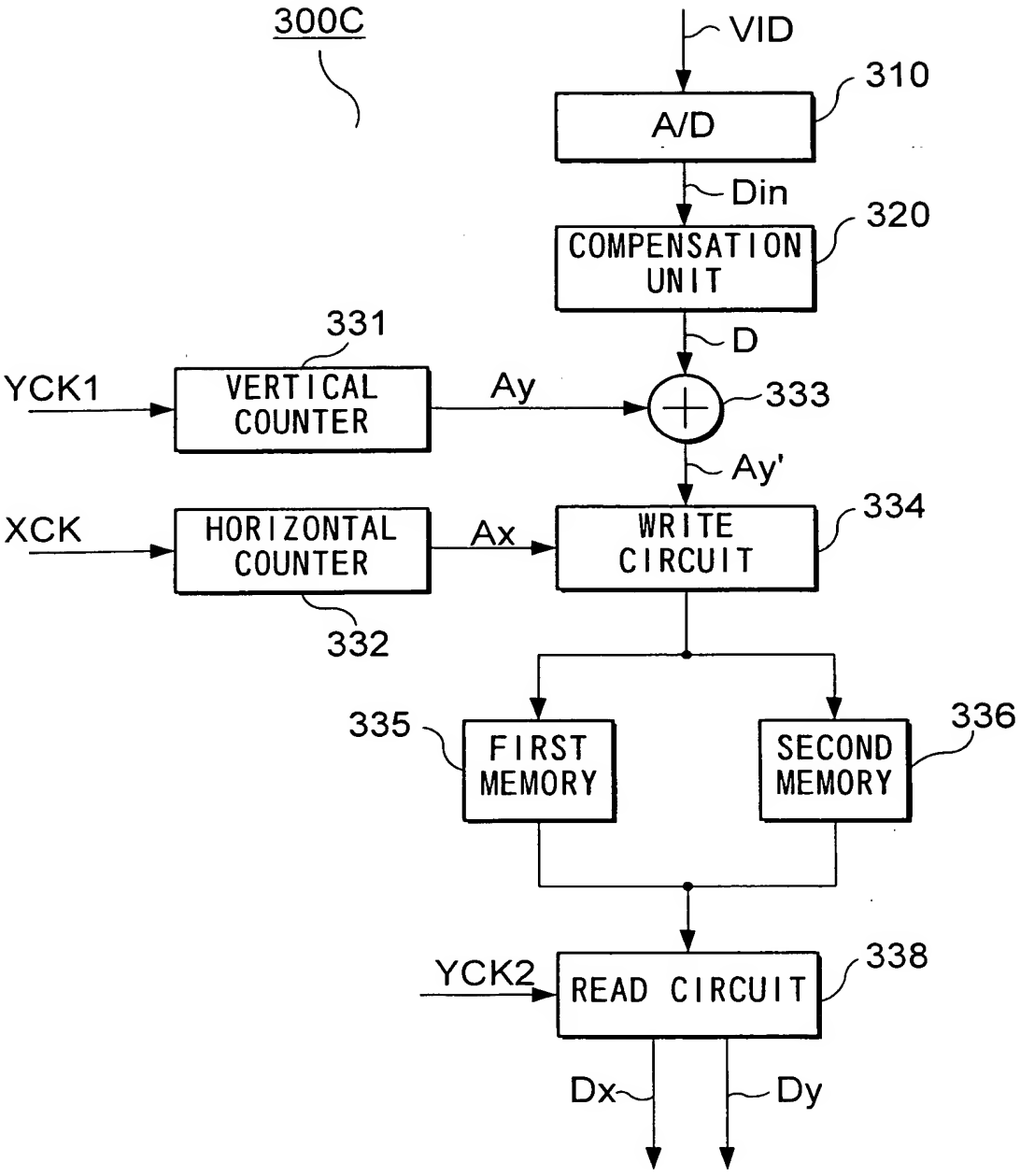
300C
VID
310
A/D
Din
320
COMPENSATION UNIT
D
331
YCK1
VERTICAL COUNTER
Ay
333
Ay'
XCK
HORIZONTAL COUNTER
Ax
WRITE CIRCUIT
334
332
335
FIRST MEMORY
SECOND MEMORY
336
YCK2
READ CIRCUIT
338
Dx
Dy

FIG. 34

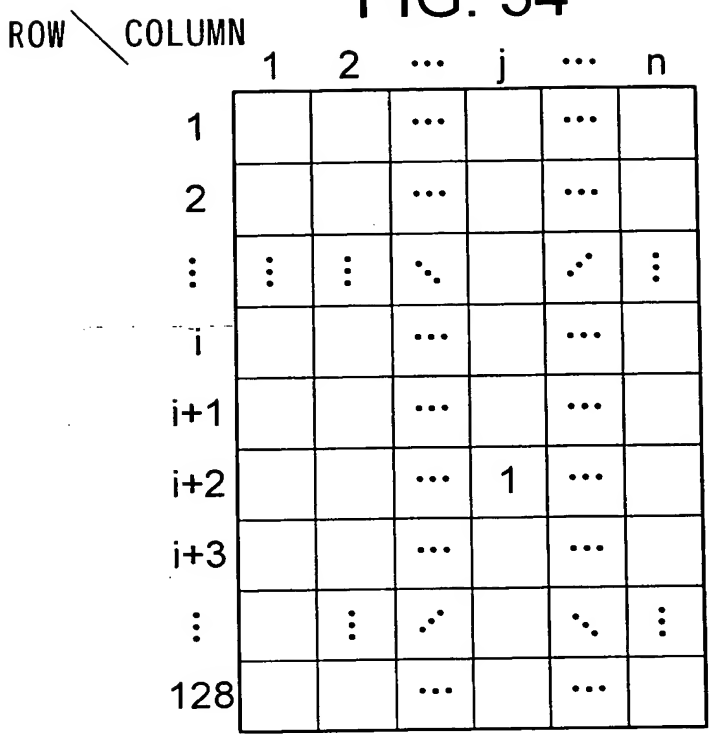
ROW
COLUMN
1
2
j
n
i
i+1
i+2
i+3
128
1

FIG. 35

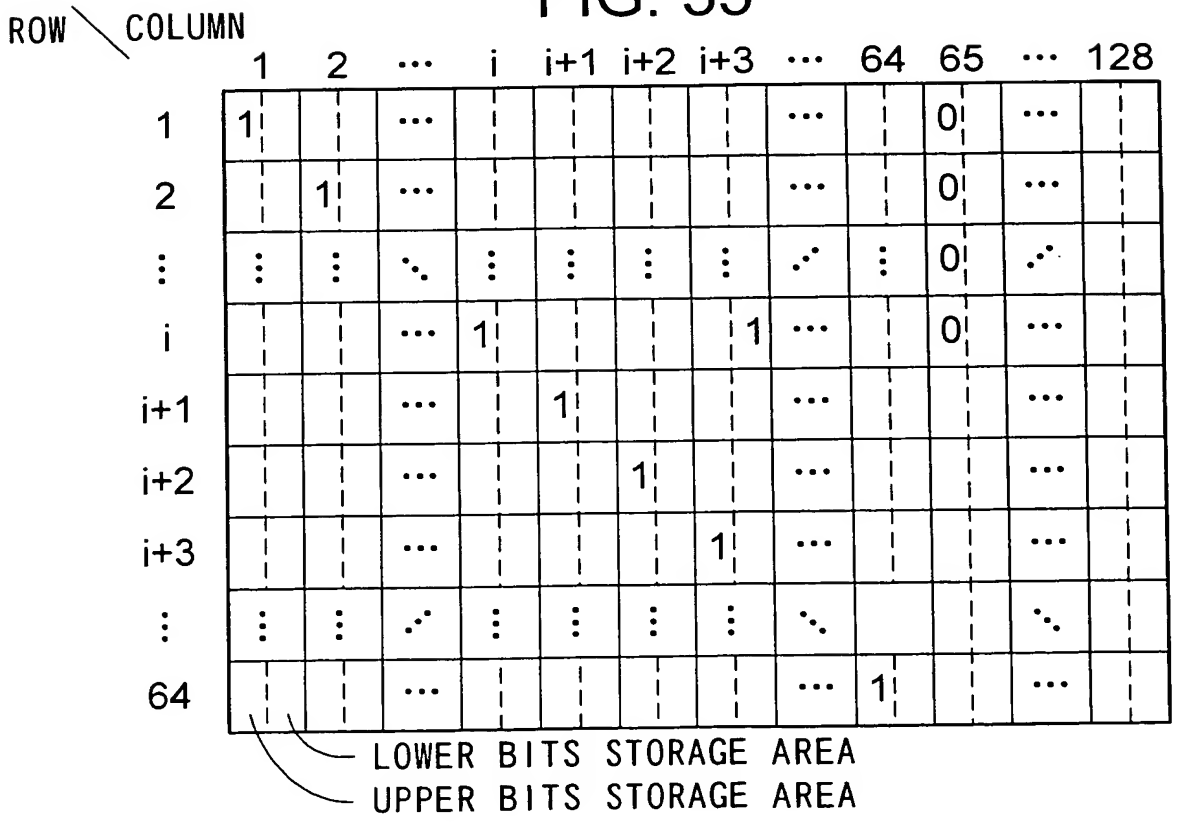
ROW
COLUMN
1
2
i
i+1
i+2
i+3
64
65
128
0
LOWER BITS STORAGE AREA
UPPER BITS STORAGE AREA

FIG. 36

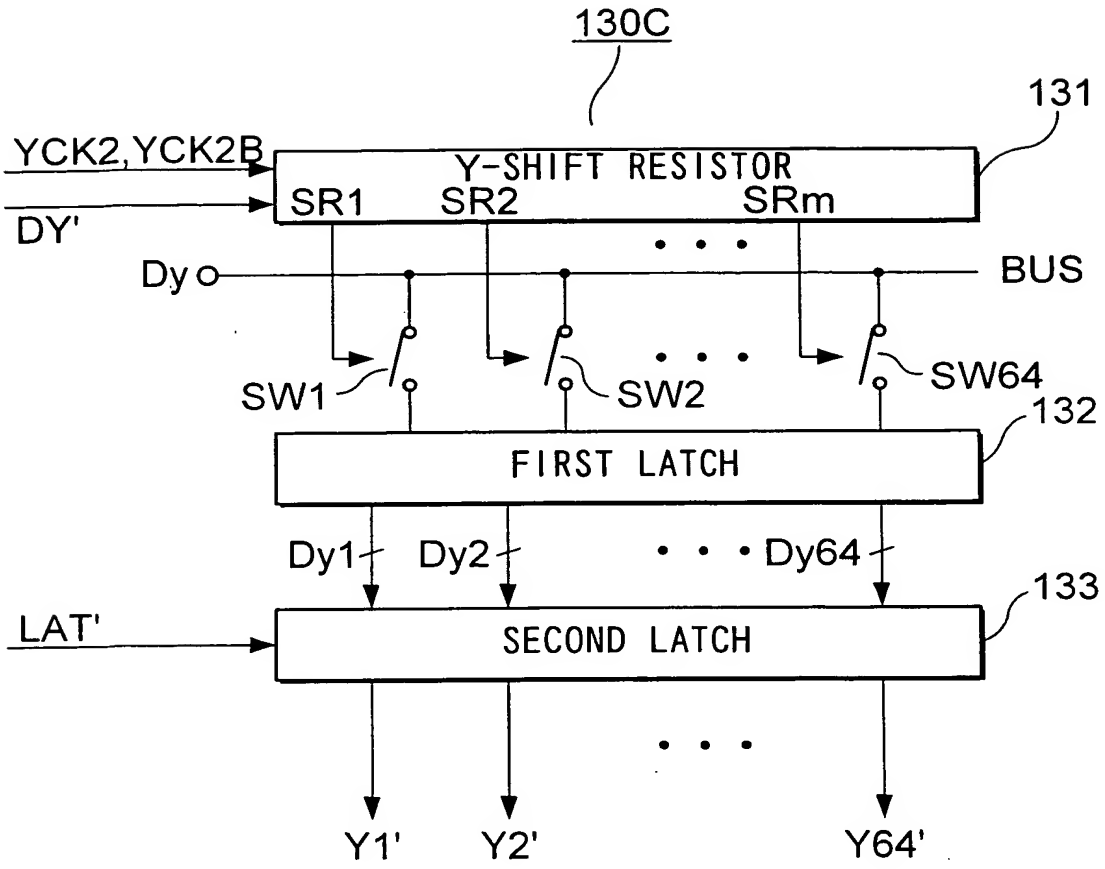
130C
131
YCK2,YCK2B
DY'
Y-SHIFT RESISTOR
SR1
SR2
SRm
Dy
BUS
SW1
SW2
SW64
132
FIRST LATCH
Dy1
Dy2
Dy64
133
LAT'
SECOND LATCH
Y1'
Y2'
Y64'

FIG. 37

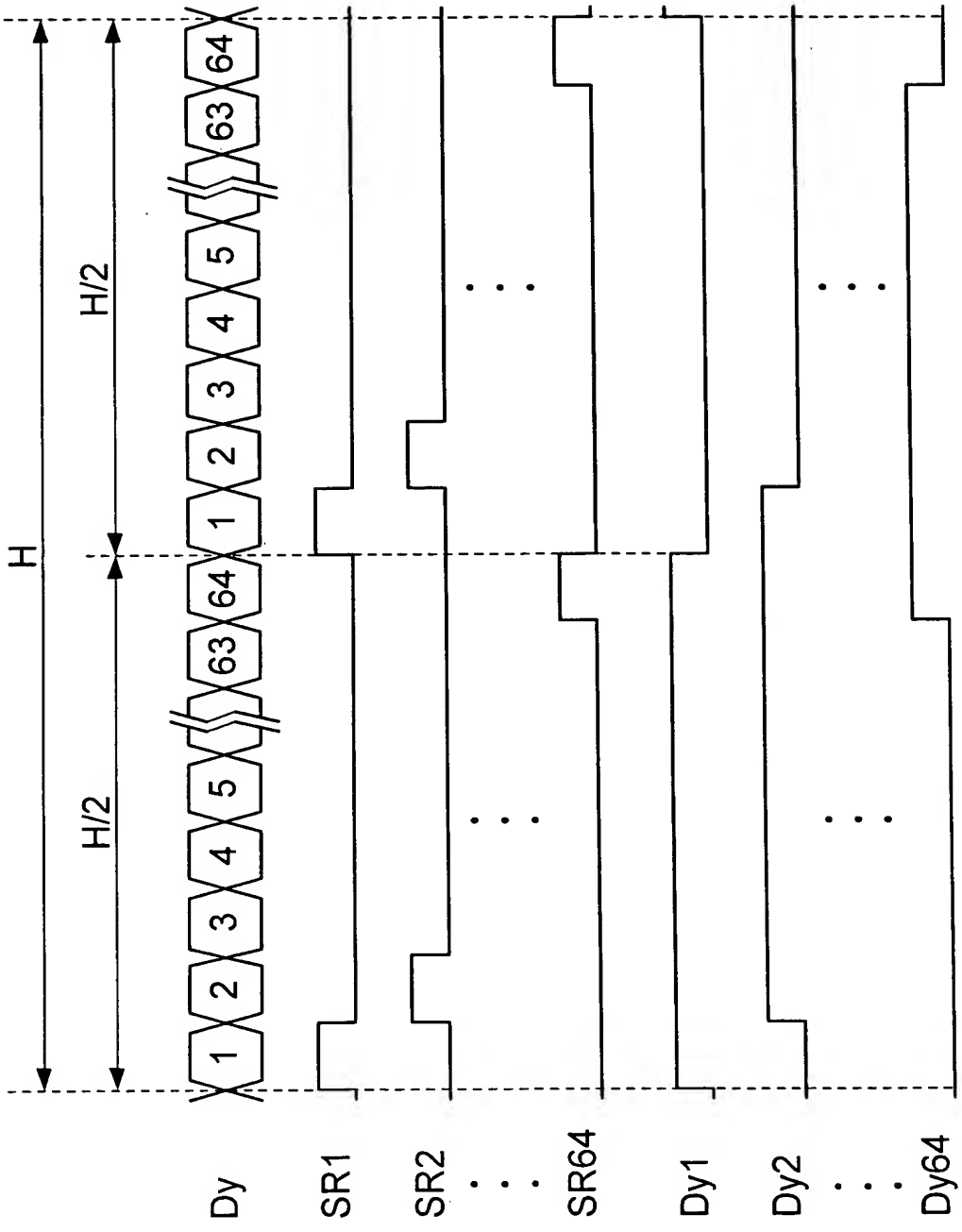

FIG. 38

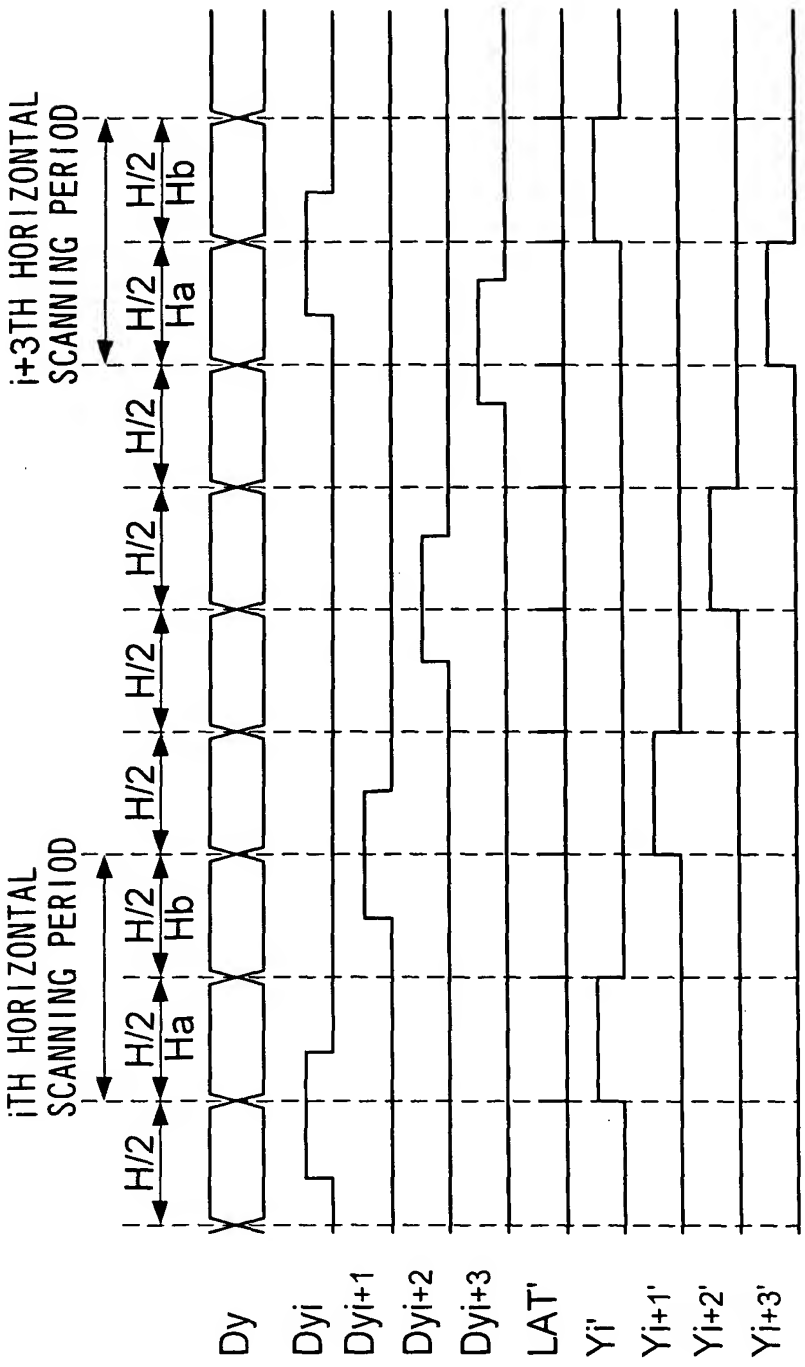
iTH HORIZONTAL SCANNING PERIOD
i+3TH HORIZONTAL SCANNING PERIOD
H/2
Ha
Hb
Dy
Dyi
Dyi+1
Dyi+2
Dyi+3
LAT'
Yi'
Yi+1'
Yi+2'
Yi+3'

FIG. 39

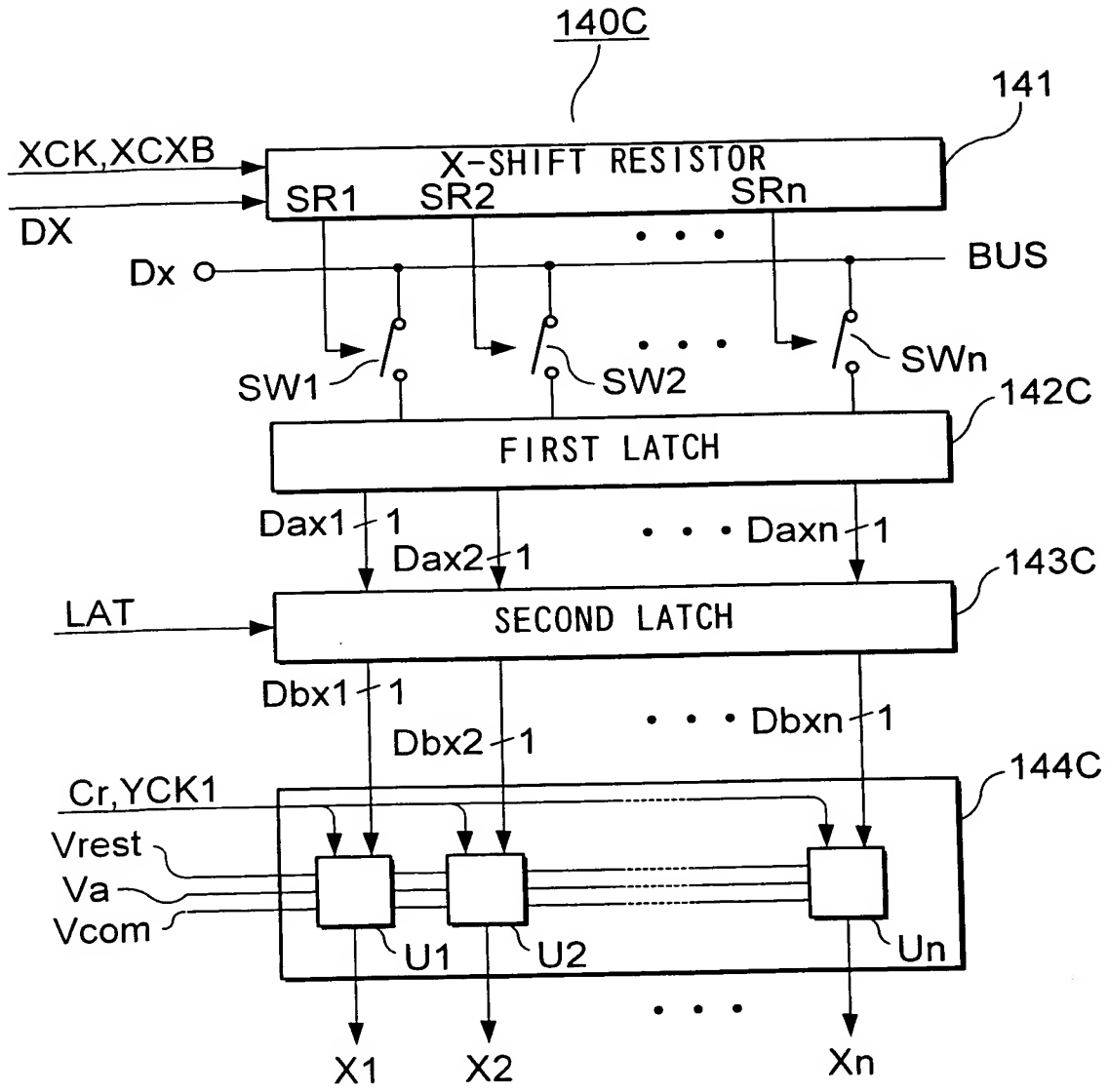
140C
141
XCK,XCXB
X-SHIFT RESISTOR
SR1
SR2
SRn
DX
Dx
BUS
SW1
SW2
SWn
142C
FIRST LATCH
Dax1
Dax2
Daxn
143C
LAT
SECOND LATCH
Dbx1
Dbx2
Dbxn
144C
Cr,YCK1
Vrest
Va
Vcom
U1
U2
Un
X1
X2
Xn

FIG. 40

Cr	YCK1	Dbj	Xj
L	L	L	HIGH-IMPEDANCE
L	L	H	Vcom
L	H	L	Va
L	H	H	Va
H	L	L	Vrest
H	L	H	Vrest
H	H	L	Vrest
H	H	H	Vrest

FIG. 41

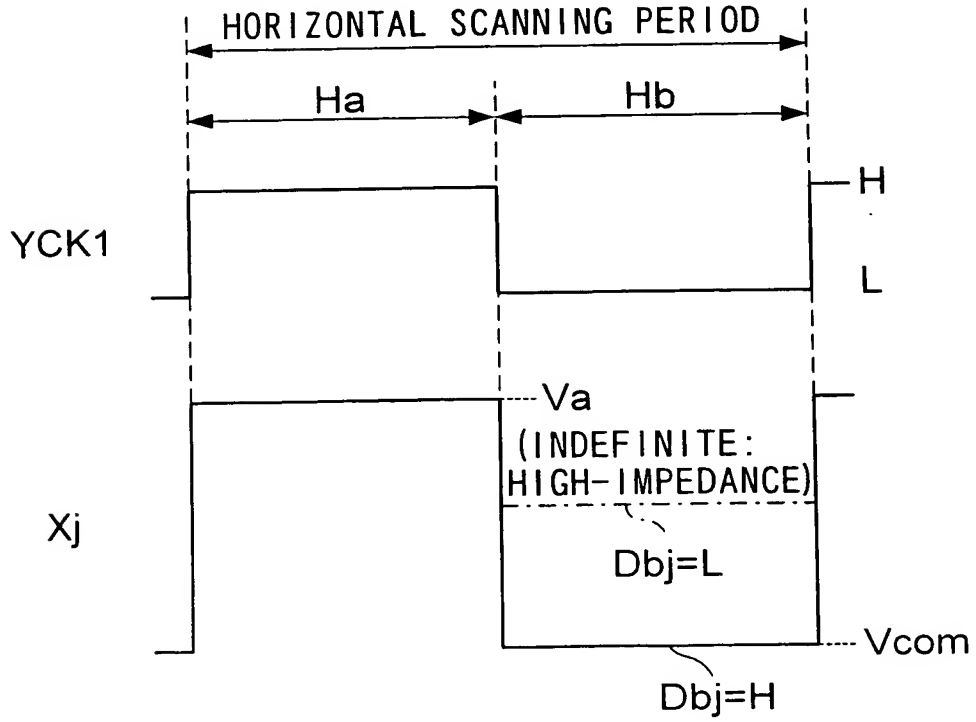

FIG. 42

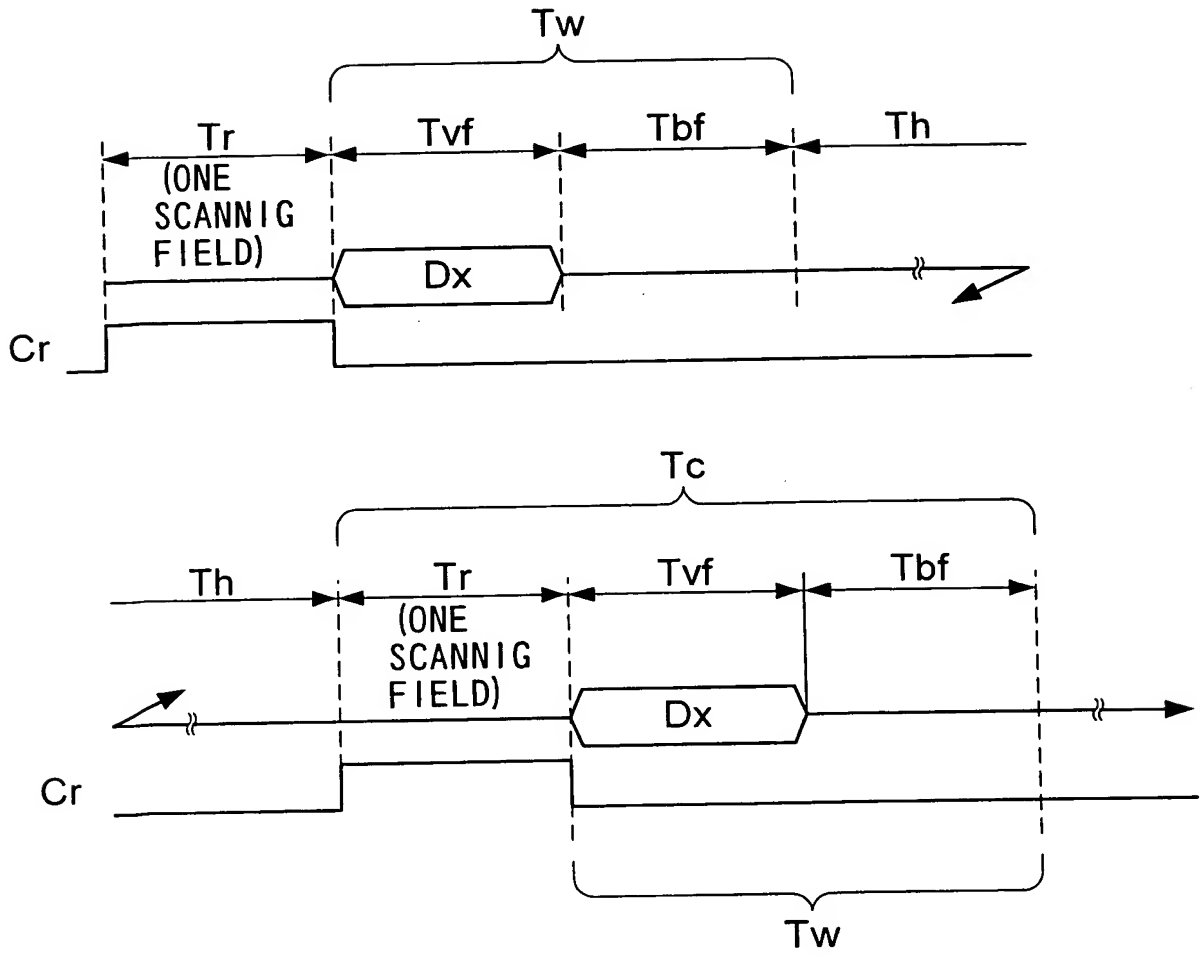
Tw
Tr
Tvf
Tbf
Th
(ONE SCANNIG FIELD)
Dx
Cr
Tc
Th
Tr
Tvf
Tbf
(ONE SCANNIG FIELD)
Dx
Cr
Tw

FIG. 43

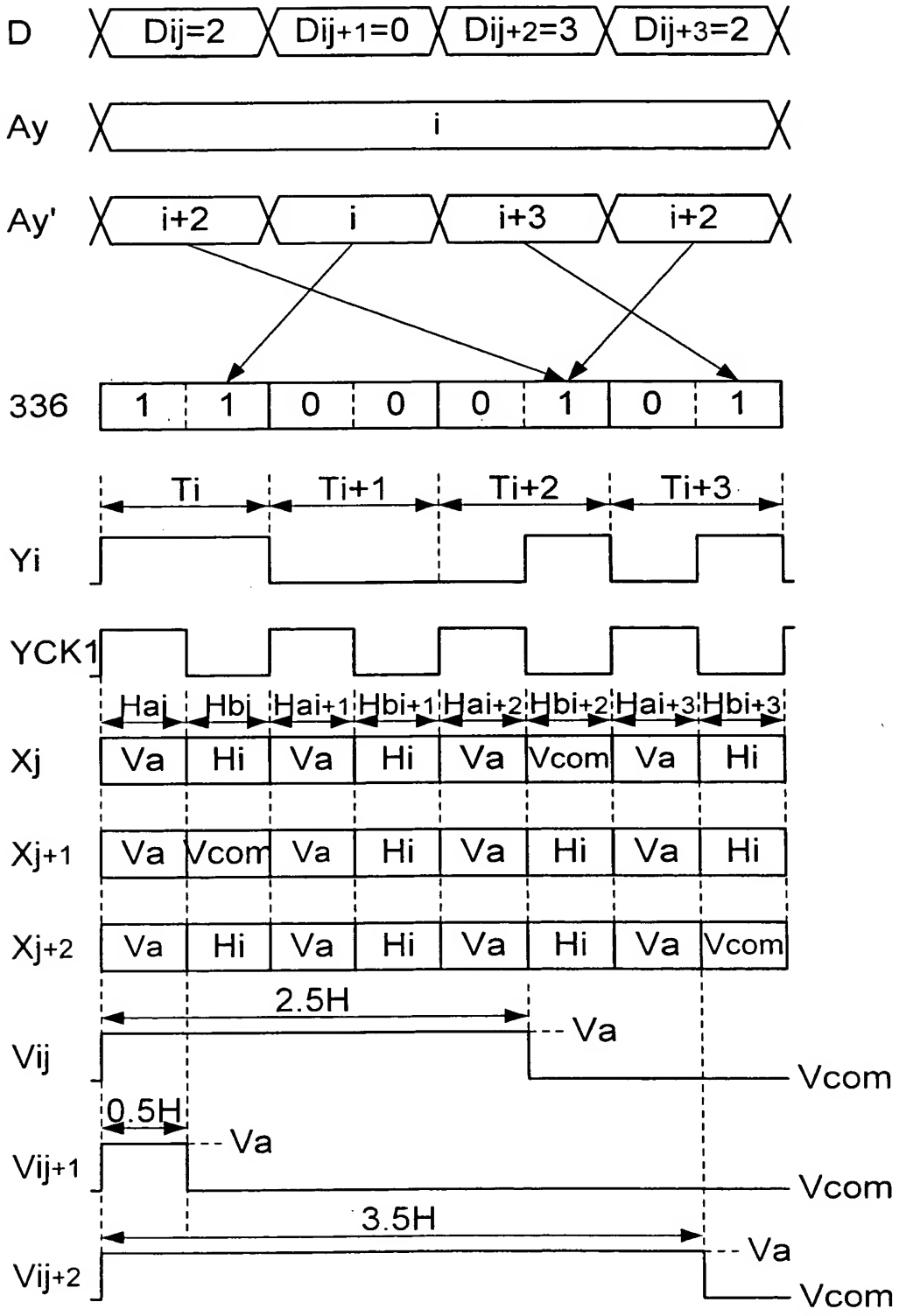
D
Dij=2
Dij+1=0
Dij+2=3
Dij+3=2
Ay
i
Ay'
i+2
i
i+3
i+2
336
1 1 0 0 0 1 0 1
Ti
Ti+1
Ti+2
Ti+3
Yi
YCK1
Hai
Hbi
Hai+1
Hbi+1
Hai+2
Hbi+2
Hai+3
Hbi+3
Xj
Va Hi Va Hi Va Vcom Va Hi
Xj+1
Va Vcom Va Hi Va Hi Va Hi
Xj+2
Va Hi Va Hi Va Hi Va Vcom
2.5H
Va
Vij
Vcom
0.5H
Va
Vij+1
Vcom
3.5H
Va
Vij+2
Vcom

FIG. 44

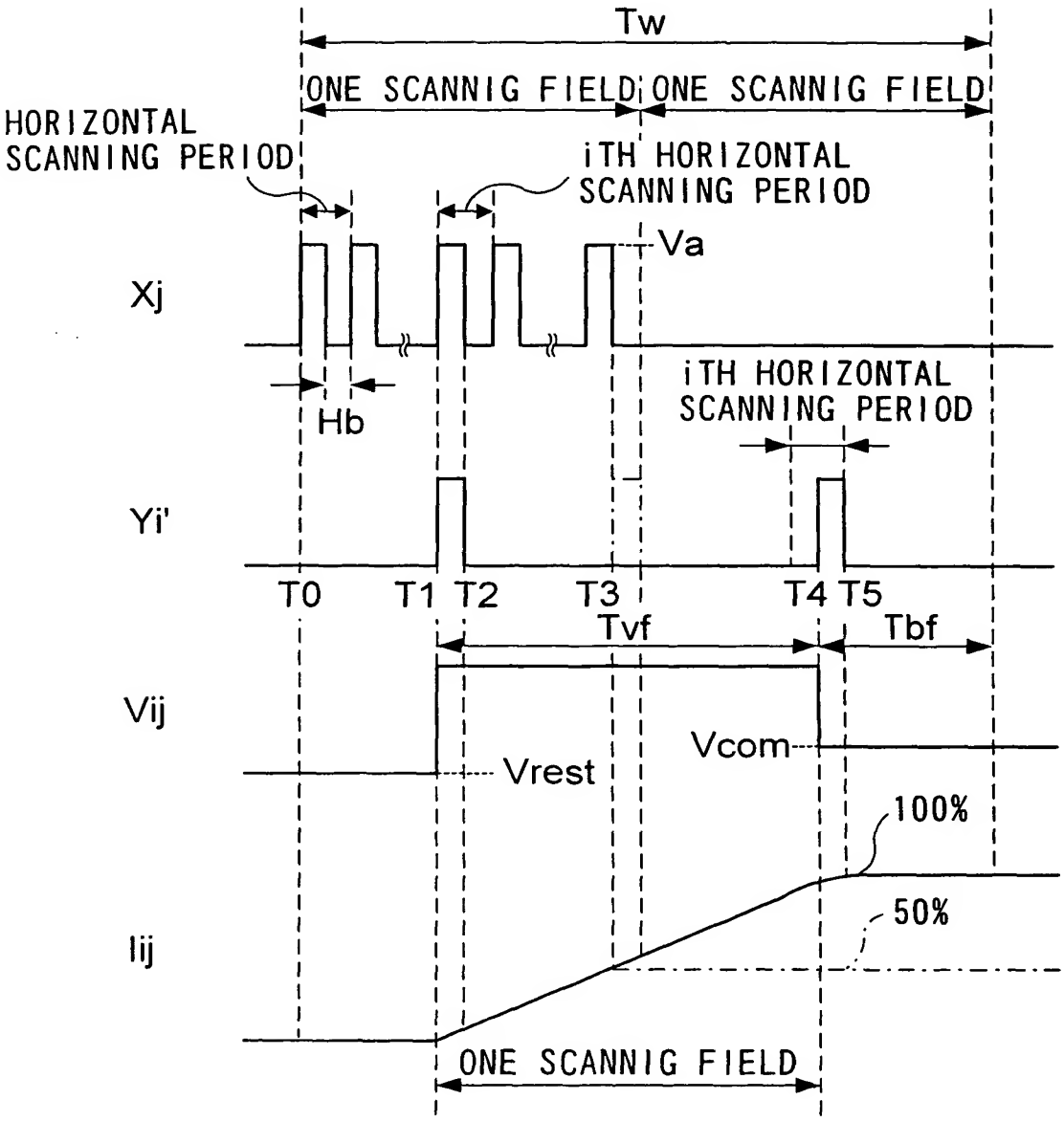
Tw
ONE SCANNIG FIELD
ONE SCANNIG FIELD
HORIZONTAL SCANNING PERIOD
iTH HORIZONTAL SCANNING PERIOD
Va
Xj
Hb
iTH HORIZONTAL SCANNING PERIOD
Yi'
T0
T1
T2
T3
T4
T5
Tvf
Tbf
Vij
Vcom
Vrest
100%
50%
Iij
ONE SCANNIG FIELD

FIG. 45

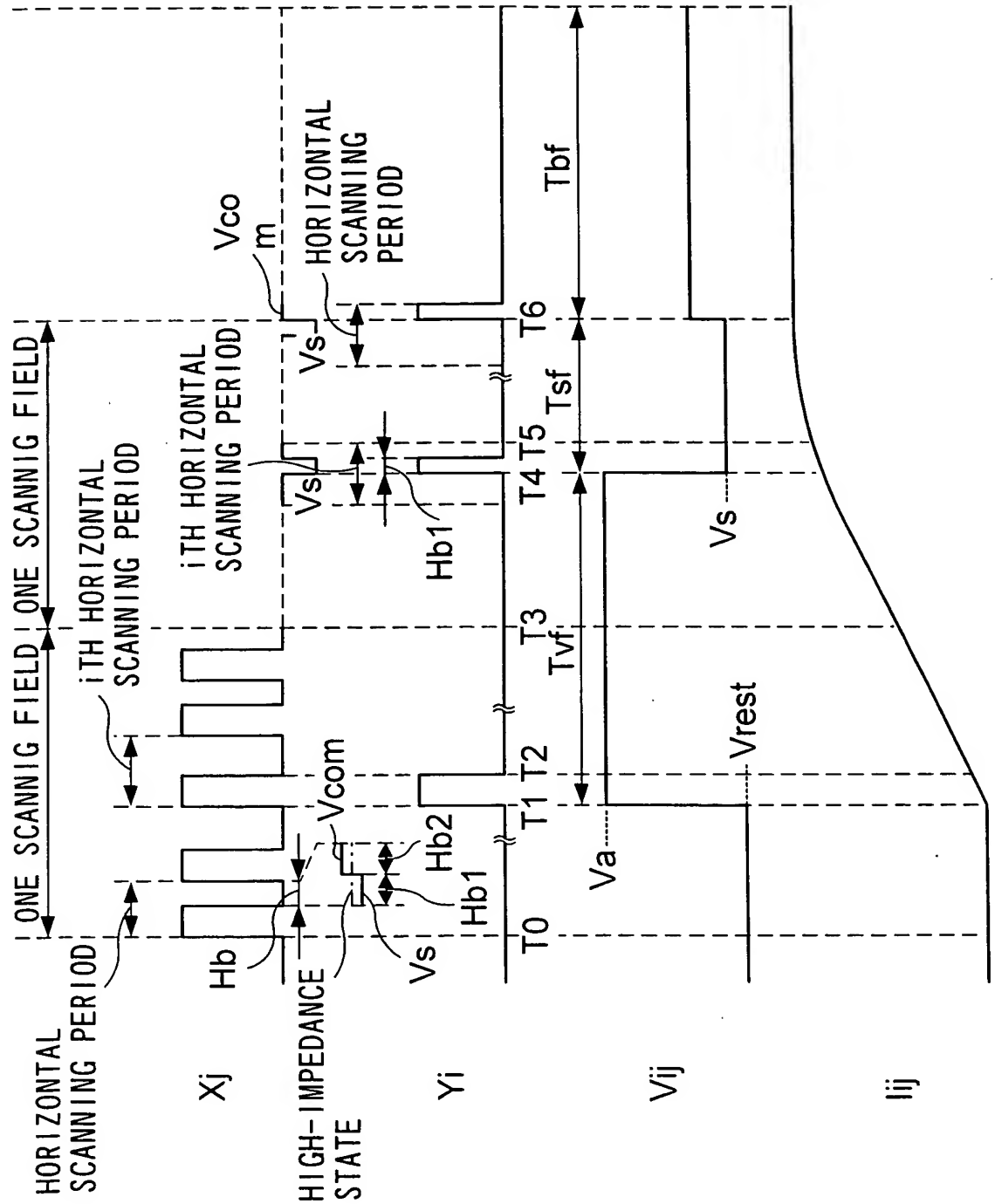
ONE SCANNIG FIELD
ONE SCANNIG FIELD
HORIZONTAL SCANNING PERIOD
iTH HORIZONTAL SCANNING PERIOD
iTH HORIZONTAL SCANNING PERIOD
HORIZONTAL SCANNING PERIOD
Vcom
Hb
Vs
Hb2
Hb1
Vs
Vs
Hb1
Vs
Vs
Va
Vrest
Vcom
HIGH-IMPEDANCE STATE
T0
T1
T2
T3
T4
T5
T6
Tvf
Tsf
Tbf
Xj
Yi
Vij
Iij

FIG. 46

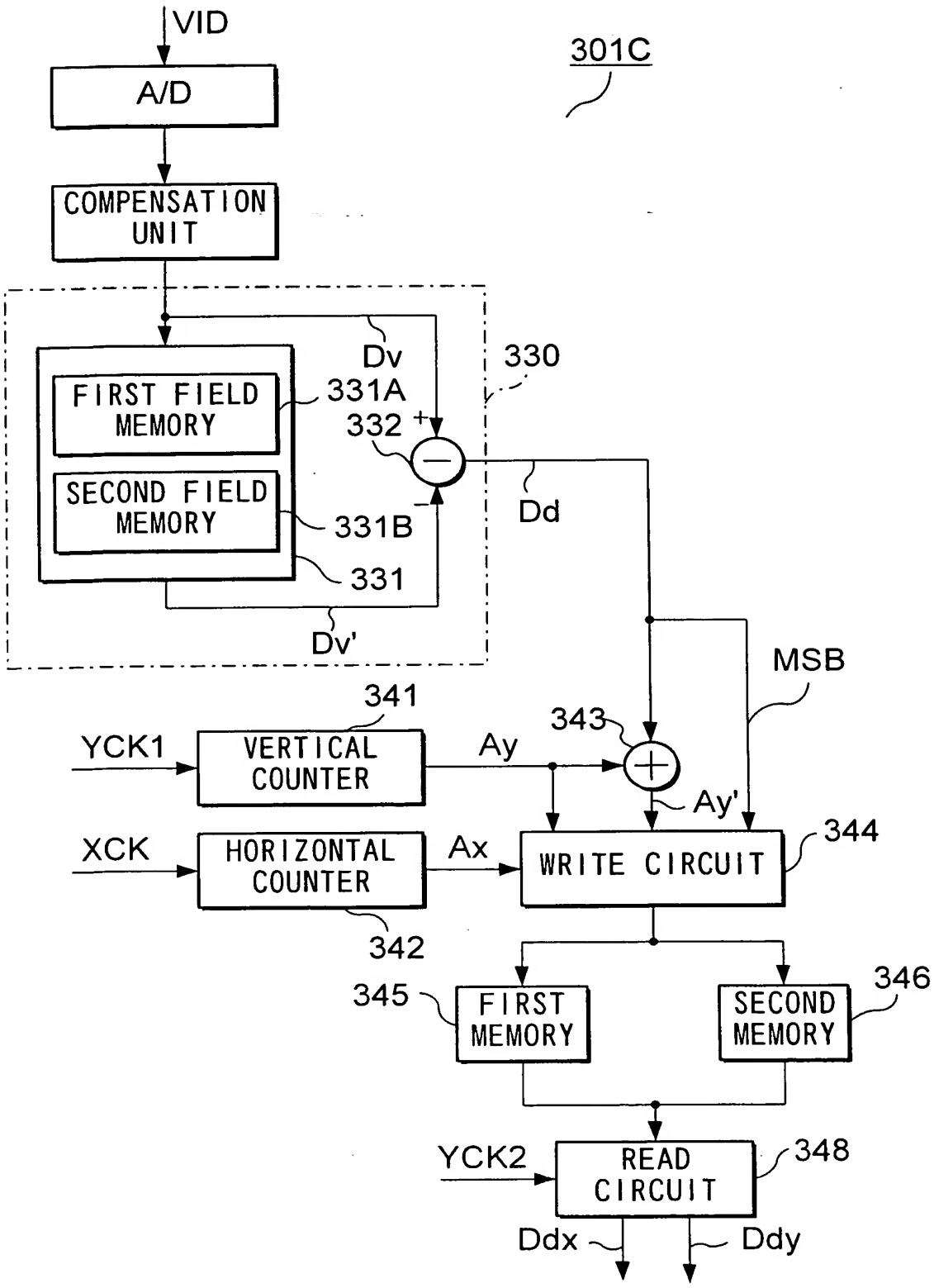
VID
A/D
COMPENSATION UNIT
301C
330
Dv
FIRST FIELD MEMORY
331A
332
SECOND FIELD MEMORY
331B
331
Dd
Dv'
MSB
341
YCK1
VERTICAL COUNTER
Ay
343
Ay'
XCK
HORIZONTAL COUNTER
Ax
WRITE CIRCUIT
344
342
345
FIRST MEMORY
SECOND MEMORY
346
YCK2
READ CIRCUIT
348
Ddx
Ddy

FIG. 47

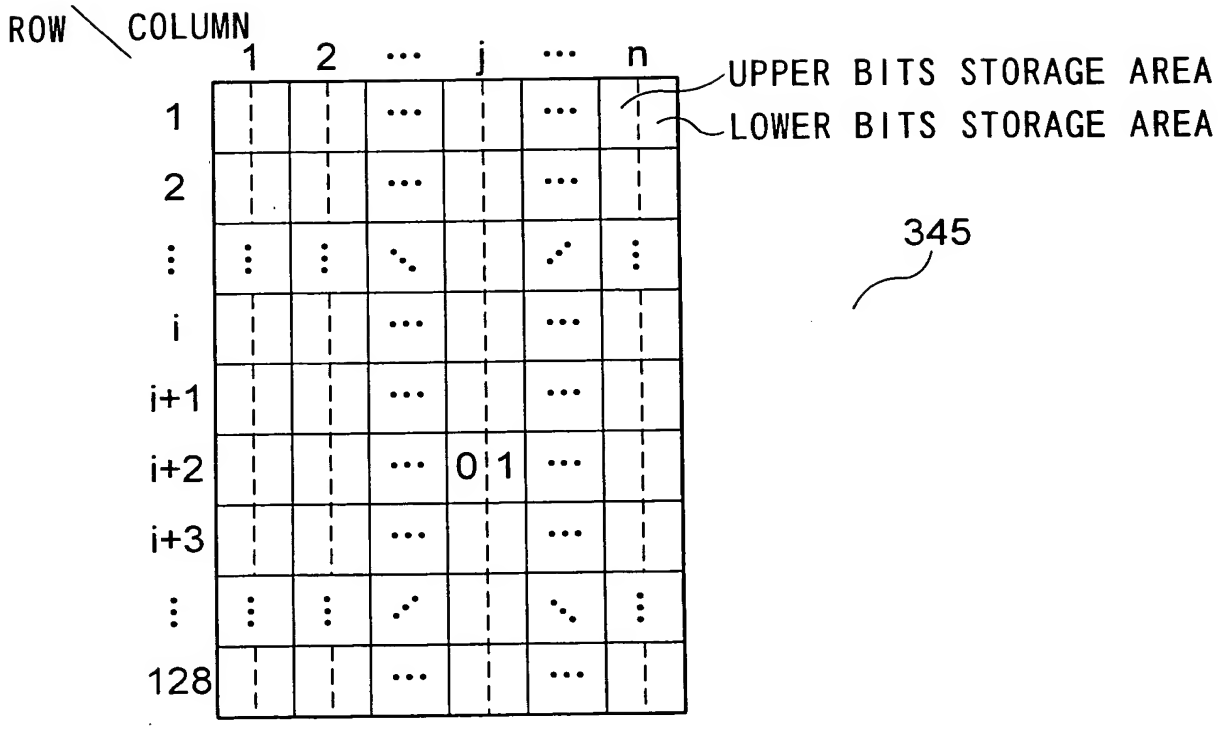
ROW
COLUMN
1
2
...
j
...
n
1
2
i
i+1
i+2
i+3
128
0
1
UPPER BITS STORAGE AREA
LOWER BITS STORAGE AREA
345

FIG. 48

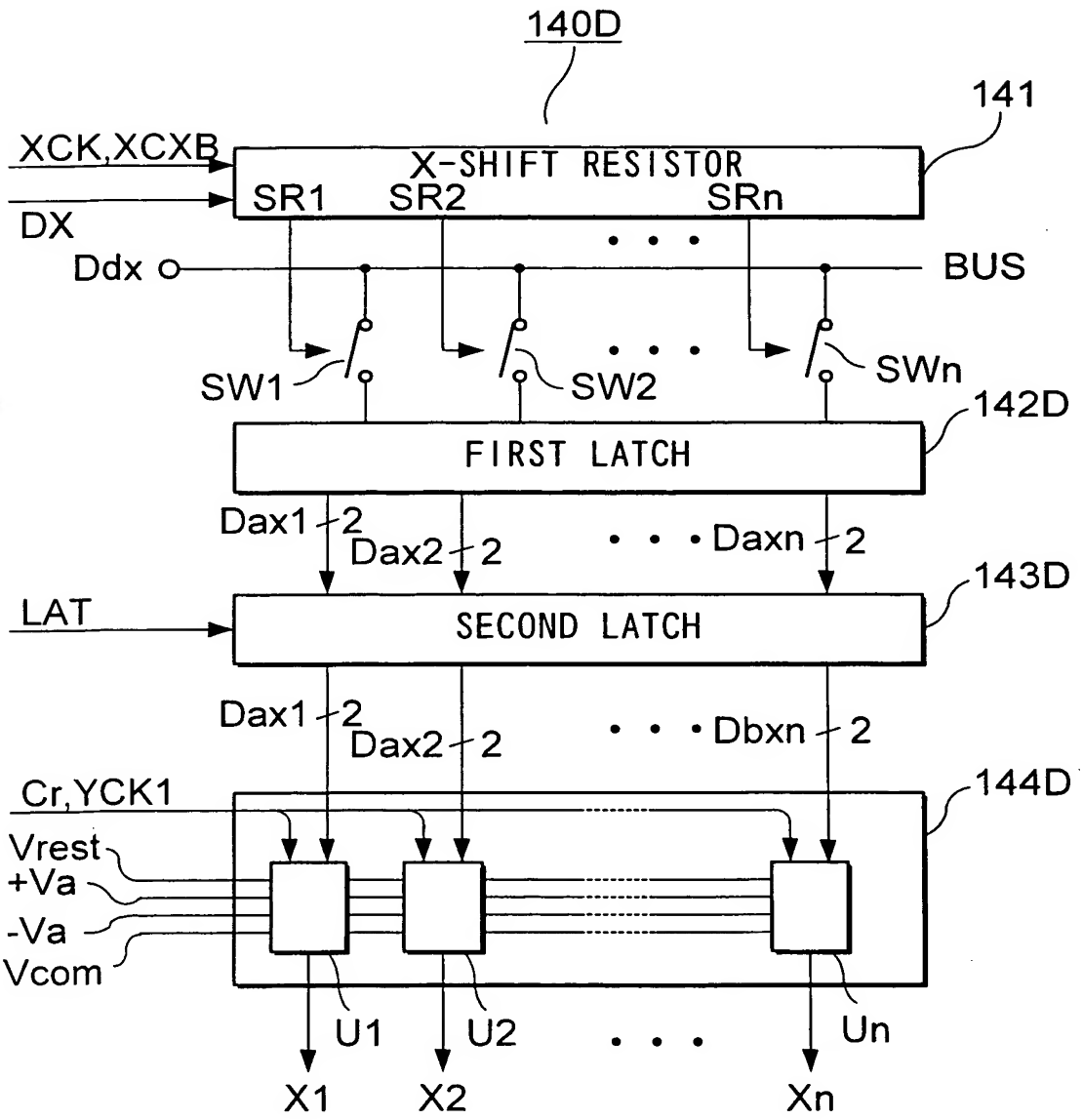
140D
141
XCK,XCXB
X-SHIFT RESISTOR
SR1
SR2
SRn
DX
Ddx
BUS
SW1
SW2
SWn
142D
FIRST LATCH
Dax1
2
Dax2
2
Daxn
2
143D
LAT
SECOND LATCH
Dax1
2
Dax2
2
Dbxn
2
144D
Cr,YCK1
Vrest
+Va
-Va
Vcom
U1
U2
Un
X1
X2
Xn

FIG. 49

Cr	YCK1	Ddbj		Xj
		LOWER BITS	UPPER BITS	
L	L	L	L or H	HIGH-IMPEDANCE
L	L	H	L or H	Vcom
L	H	L	L (0)	+Va
			H (1)	-Va
L	H	H	L (0)	+Va
			H (1)	-Va
H	L	L	L or H	Vrest
H	L	H	L or H	Vrest
H	H	L	L or H	Vrest
H	H	H	L or H	Vrest

FIG. 50

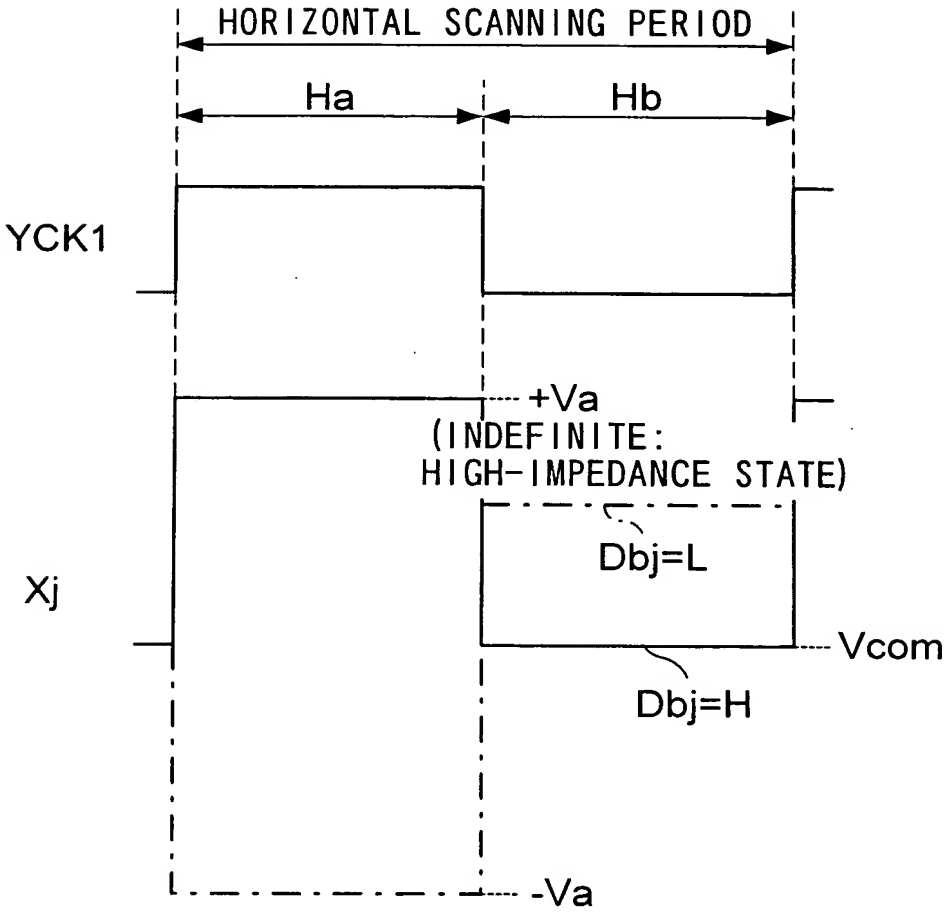
HORIZONTAL SCANNING PERIOD
Ha
Hb
YCK1
+Va
(INDEFINITE:
HIGH-IMPEDANCE STATE)
Dbj=L
Xj
Vcom
Dbj=H
-Va

FIG. 51

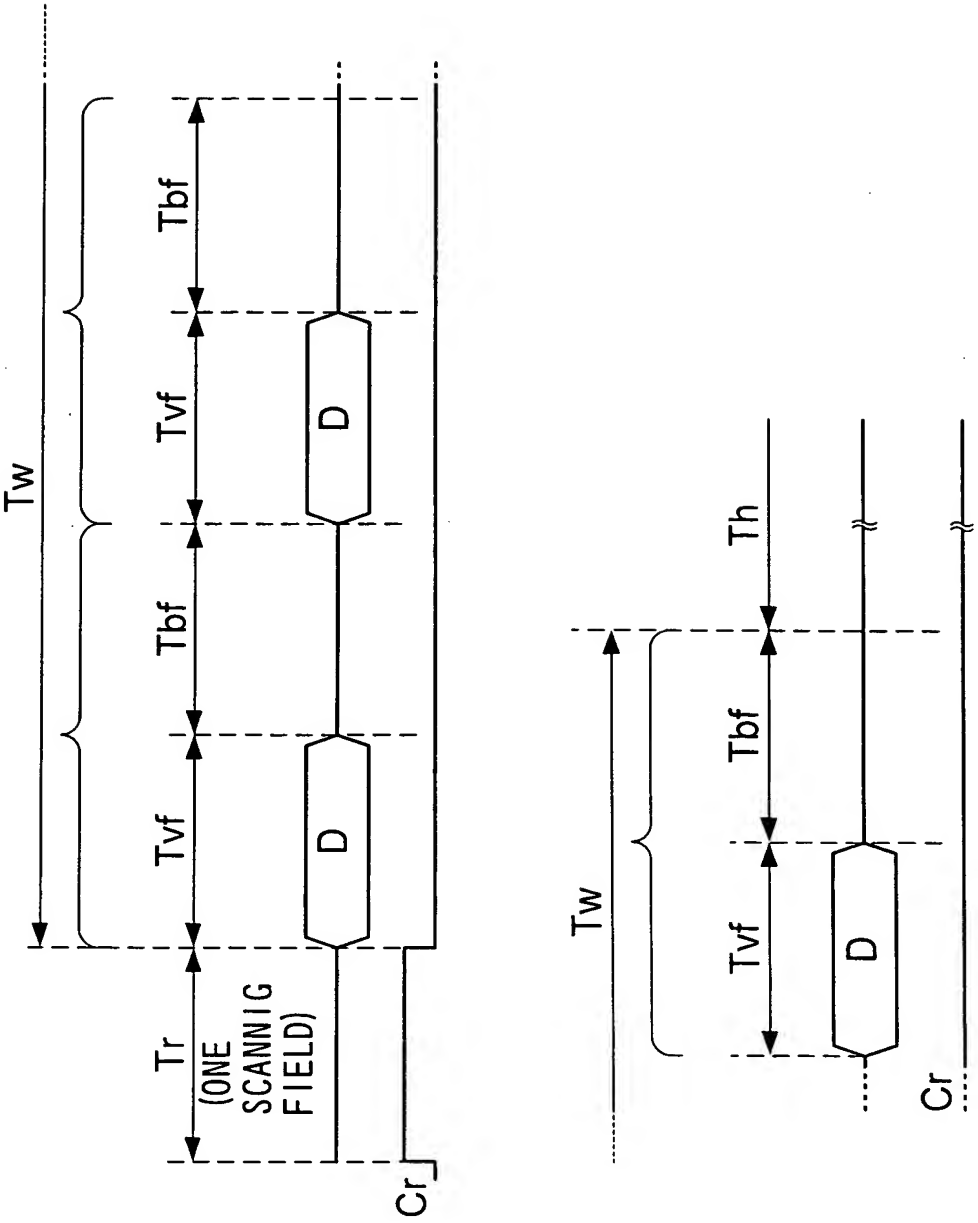

FIG. 52

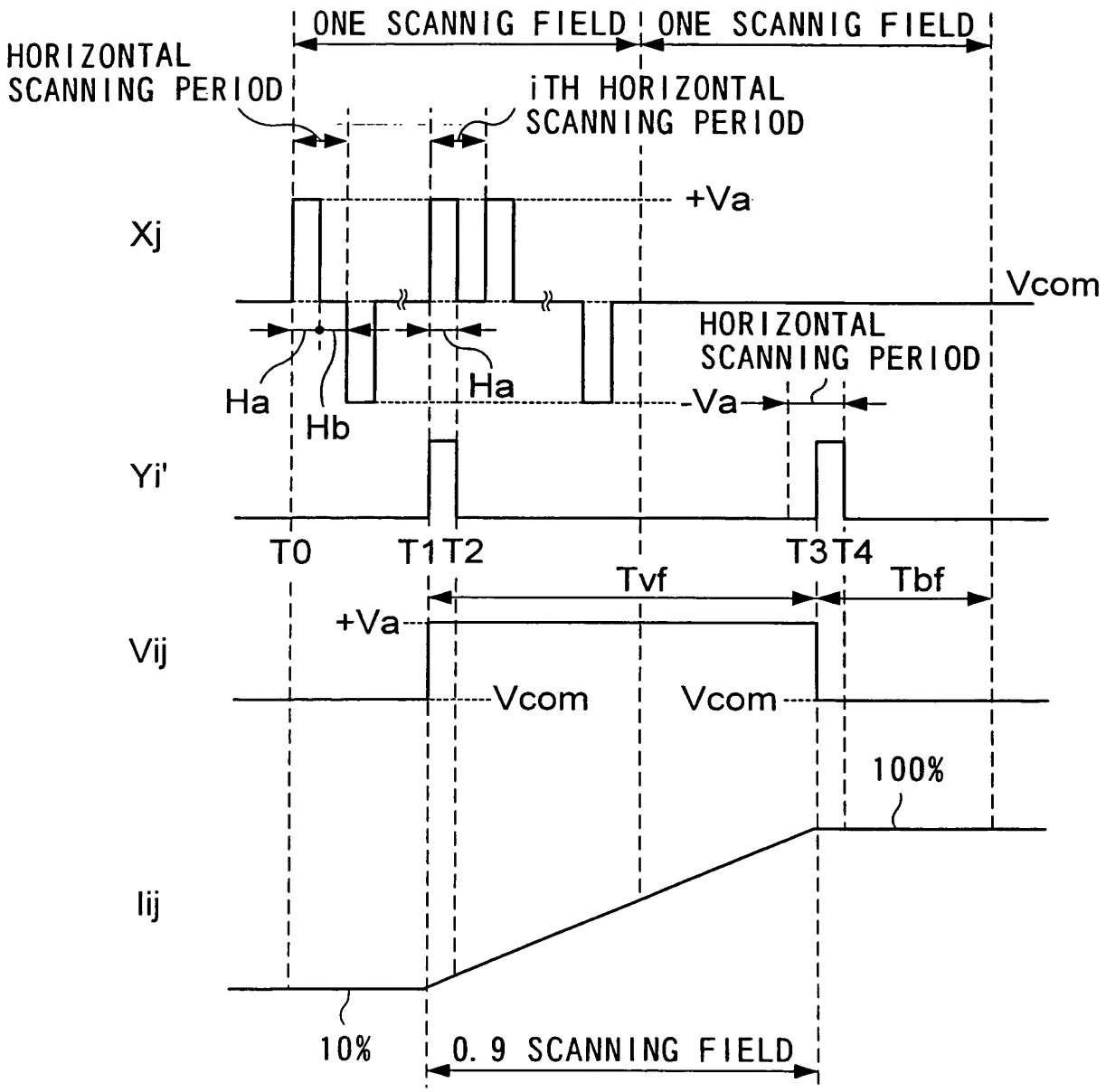
ONE SCANNIG FIELD
ONE SCANNIG FIELD
HORIZONTAL SCANNING PERIOD
iTH HORIZONTAL SCANNING PERIOD
Xj
+Va
Vcom
HORIZONTAL SCANNING PERIOD
Ha
Hb
Ha
-Va
Yi'
T0
T1
T2
T3
T4
Tvf
Tbf
Vij
+Va
Vcom
Vcom
100%
Iij
10%
0.9 SCANNING FIELD

FIG. 53

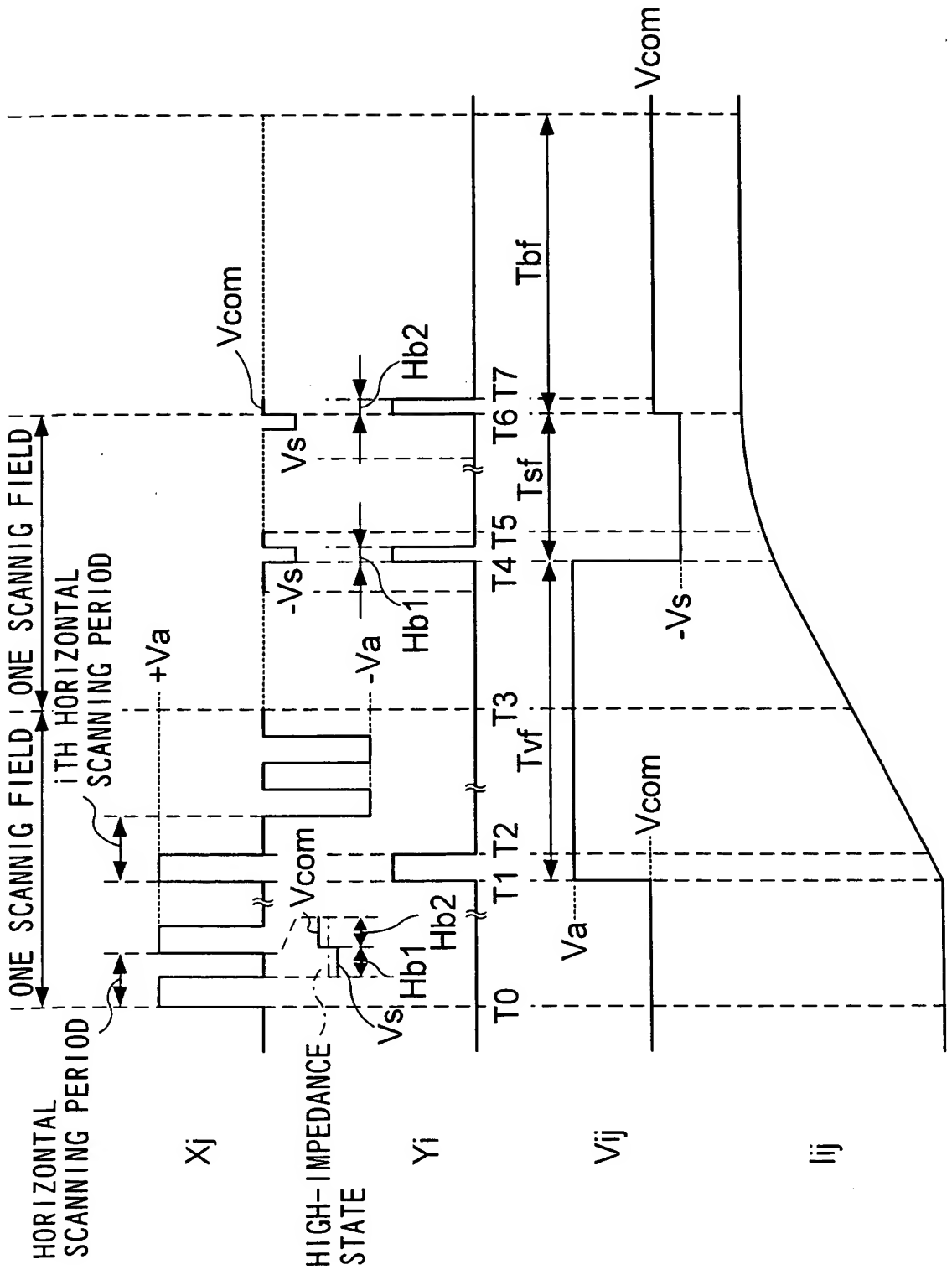
ONE SCANNIG FIELD
ONE SCANNIG FIELD
HORIZONTAL SCANNING PERIOD
iTH HORIZONTAL SCANNING PERIOD
HIGH-IMPEDANCE STATE
Xj
Yi
Vij
Iij
Vcom
+Va
-Va
Vs
-Vs
Hb1
Hb2
T0
T1
T2
T3
T4
T5
T6
T7
Tvf
Tsf
Tbf

FIG. 54

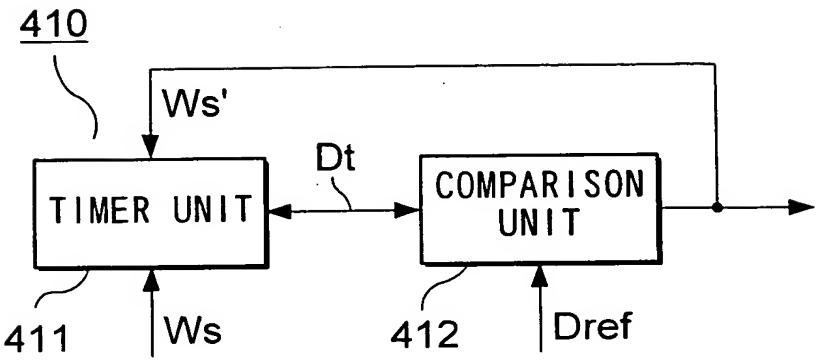
410
Ws'
Dt
TIMER UNIT
COMPARISON UNIT
411
Ws
412
Dref

FIG. 55

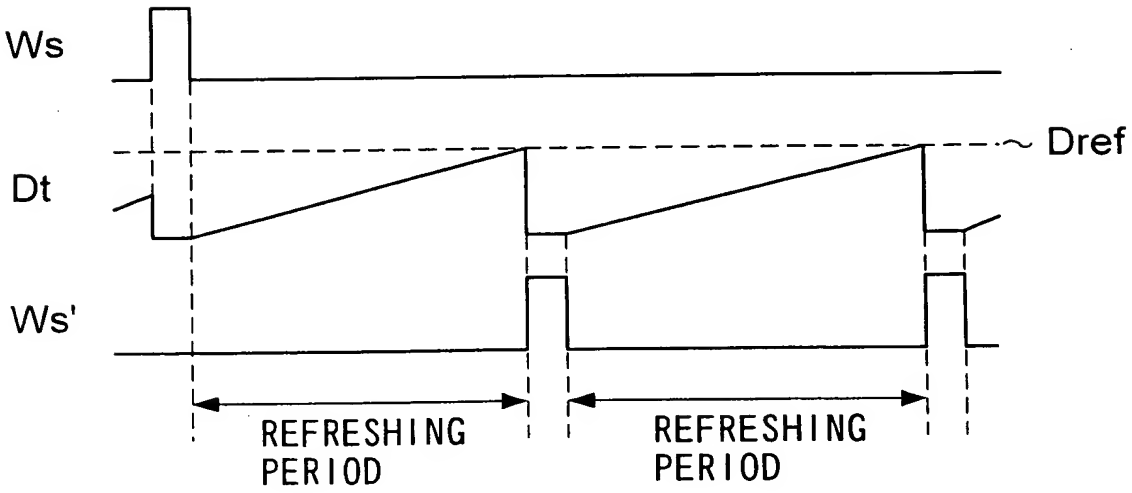
Ws
Dref
Dt
Ws'
REFRESHING PERIOD
REFRESHING PERIOD

FIG. 56

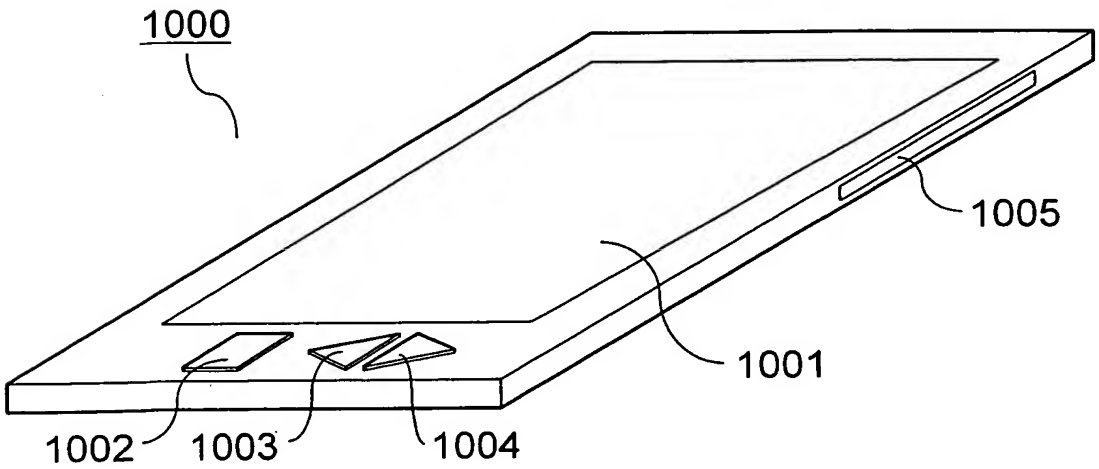

FIG. 57

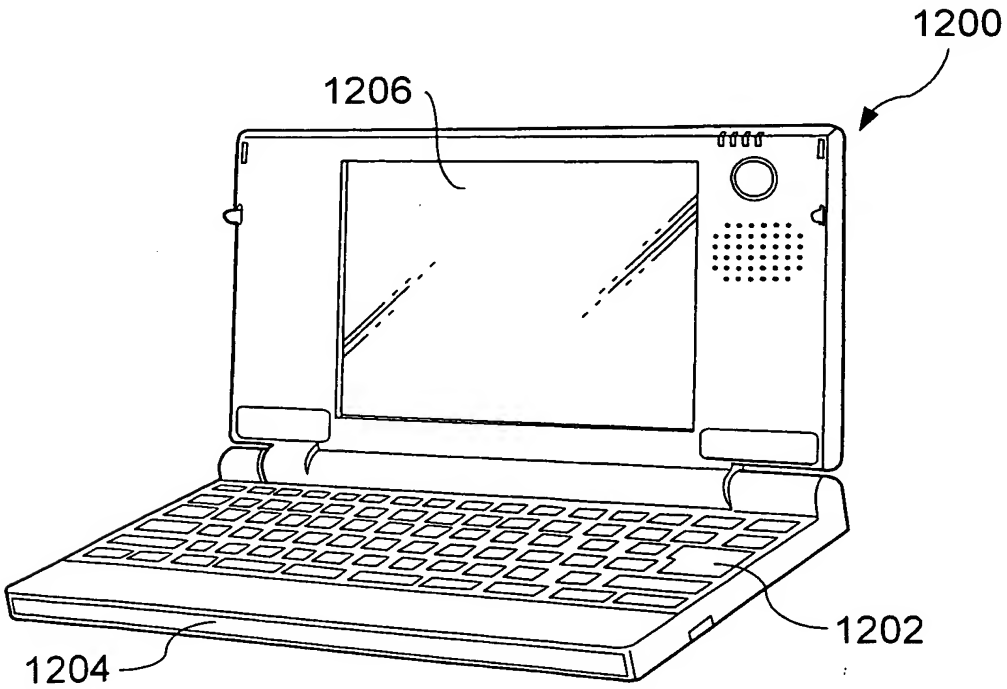

FIG. 58